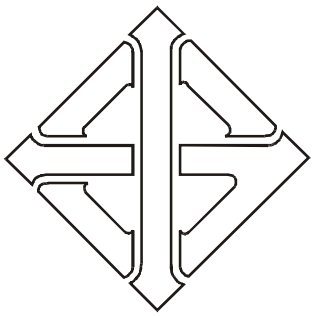

มาตรฐานผลิตภัณฑ์อุตสาหกรรม

THAI INDUSTRIAL STANDARD

มอก. 1972 – 2552

IEC 60747 – 6(2000 – 12)

อุปกรณ์สารกึ่งตัวนำ

เล่ม 6 ไทริสเตอร์

SEMICONDUCTOR DEVICES-

PART 6 : THYRISTORS

สำนักงานมาตรฐานผลิตภัณฑ์อุตสาหกรรม

กระทรวงอุตสาหกรรม

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มาตรฐานผลิตภัณฑ์อุตสาหกรรม

อุปกรณ์สารกึ่งตัวนำ

เล่ม 6 ไทริสเตอร์

มอก. 1972–2552

สำนักงานมาตรฐานผลิตภัณฑ์อุตสาหกรรม
กระทรวงอุตสาหกรรม ถนนพระรามที่ 6 กรุงเทพฯ 10400
โทรศัพท์ 02 202 3300

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วันที่ 14 ธันวาคม พุทธศักราช 2553

มาตรฐานผลิตภัณฑ์อุตสาหกรรมอุปกรณ์สารกึ่งตัวนำอุปกรณ์ไม่รวมหน่วยและวงจรรวม เล่ม 6 ไทริสเตอร์ ได้ประกาศใช้ครั้งแรกโดยรับ IEC 747-6 (1983) Semiconductor Devices - Discrete devices and integrated circuits - Part 6: Tyristors มาใช้ในระดับเหมือนกันทุกประการ (Identical) โดยใช้ IEC ฉบับภาษาอังกฤษเป็นหลัก โดยประกาศในราชกิจจานุเบกษา ฉบับประกาศทั่วไป เล่มที่118 ตอนที่ 90ง วันที่ 8 พฤศจิกายน พุทธศักราช 2544

เนื่องจาก IEC ได้แก้ไขปรับปรุงมาตรฐาน IEC 747-6 (1983) เป็น IEC 60747-6 (2000) จึงได้ยกเลิกมาตรฐานเดิมและกำหนดมาตรฐานใหม่โดยรับ IEC 60747-6 (2000) Semiconductor Devices- Part 6: Thyristors มาใช้ในระดับเหมือนกันทุกประการโดยใช้มาตรฐาน IEC ฉบับภาษาอังกฤษเป็นหลัก

คณะกรรมการมาตรฐานผลิตภัณฑ์อุตสาหกรรมได้พิจารณามาตรฐานนี้แล้ว เห็นสมควรเสนอรัฐมนตรีประกาศตามมาตรา 15 แห่งพระราชบัญญัติมาตรฐานผลิตภัณฑ์อุตสาหกรรม พ.ศ. 2511

ประกาศกระทรวงอุตสาหกรรม

ฉบับที่ 4243 (พ.ศ. 2553)

ออกตามความในพระราชบัญญัติมาตรฐานผลิตภัณฑ์อุตสาหกรรม

พ.ศ. 2511

เรื่อง ยกเลิกมาตรฐานผลิตภัณฑ์อุตสาหกรรม

อุปกรณ์สารกึ่งตัวนำ อุปกรณ์ไม่รวมหน่วยและวงจรรวม เล่ม 6 ไทริสเตอร์

และกำหนดมาตรฐานผลิตภัณฑ์อุตสาหกรรม

อุปกรณ์สารกึ่งตัวนำ เล่ม 6 ไทริสเตอร์

โดยที่เป็นการสมควรปรับปรุงมาตรฐานผลิตภัณฑ์อุตสาหกรรม อุปกรณ์สารกึ่งตัวนำ อุปกรณ์ไม่รวมหน่วยและวงจรรวม เล่ม 6 ไทริสเตอร์ มาตรฐานเลขที่ มอก.1972-2543

อาศัยอำนาจตามความในมาตรา 15 แห่งพระราชบัญญัติมาตรฐานผลิตภัณฑ์อุตสาหกรรม พ.ศ. 2511 รัฐมนตรีว่าการกระทรวงอุตสาหกรรมออกประกาศยกเลิกประกาศกระทรวงอุตสาหกรรม ฉบับที่ 2910 (พ.ศ.2544) ออกตามความในพระราชบัญญัติมาตรฐานผลิตภัณฑ์อุตสาหกรรม พ.ศ.2511 เรื่อง กำหนดมาตรฐานผลิตภัณฑ์อุตสาหกรรม อุปกรณ์สารกึ่งตัวนำ อุปกรณ์ไม่รวมหน่วยและวงจรรวม เล่ม 6 ไทริสเตอร์ ลงวันที่ 10 สิงหาคม พ.ศ.2544 และออกประกาศกำหนดมาตรฐานผลิตภัณฑ์อุตสาหกรรม อุปกรณ์สารกึ่งตัวนำ เล่ม 6 ไทริสเตอร์ มาตรฐานเลขที่ มอก.1972-2552 ขึ้นใหม่ ดังมีรายละเอียดต่อท้ายประกาศนี้

ทั้งนี้ให้มีผลตั้งแต่วันถัดจากวันที่ประกาศในราชกิจจานุเบกษาเป็นต้นไป

ประกาศ ณ วันที่ 31 สิงหาคม พ.ศ. 2553

ชัยวุฒิ บรรณวัฒน์

รัฐมนตรีว่าการกระทรวงอุตสาหกรรม

มาตรฐานผลิตภัณฑ์อุตสาหกรรม
อุปกรณ์สารกึ่งตัวนำ-
เล่ม 6 ไทริสเตอร์

มาตรฐานผลิตภัณฑ์อุตสาหกรรมนี้กำหนดขึ้นโดยรับ IEC 60747-6 (2000) Semiconductor Devices-Part 6 : Thyristors มาใช้ในระดับเหมือนกันทุกประการ (identical) โดยใช้ IEC ฉบับภาษาอังกฤษเป็นหลัก

มาตรฐานผลิตภัณฑ์อุตสาหกรรมนี้กำหนดมาตรฐานสำหรับอุปกรณ์สารกึ่งตัวนำแต่ละประเภทซึ่งครอบคลุมถึง

- ไทรโอด ไทริสเตอร์ปิดกั้นย้อนกลับ
- ไทรโอด ไทริสเตอร์ปิดกั้นย้อนกลับแบบไม่สมมาตร
- ไทรโอด ไทริสเตอร์นำกระแสย้อนกลับ
- ไทรโอด ไทริสเตอร์สองทิศทาง (ไทรแอก)
- ไทริสเตอร์แบบ GTO (GATE TURN-OFF)

มาตรฐานผลิตภัณฑ์อุตสาหกรรมนี้ยังไม่รวมถึงไทริสเตอร์ระงับเสิร์จและไดแอก

รายละเอียดให้เป็นไปตาม IEC 60747-6 (2000)

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IEC Central office
3, rue de Varembé,
CH-1211 Geneva 20
Switzerland
E-mail : inmail@iec.ch
Web : www.iec.ch

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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SEMICONDUCTOR DEVICES –

Part 6: Thyristors

FOREWORD

1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of the IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested National Committees.
3) The documents produced have the form of recommendations for international use and are published in the form of standards, technical specifications, technical reports or guides and they are accepted by the National Committees in that sense.
4) In order to promote international unification, IEC National Committees undertake to apply IEC International Standards transparently to the maximum extent possible in their national and regional standards. Any divergence between the IEC Standard and the corresponding national or regional standard shall be clearly indicated in the latter.
5) The IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with one of its standards.
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International Standard IEC 60747-6 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This second edition cancels and replaces the first edition, published in 1983, and its amendments 1 and 2 and constitutes a technical revision.

The text of this standard is based on the following documents:

FDIS	Report on voting
47E/155/FDIS	47E/168/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 3.

Annex A is for information only.

The committee has decided that the contents of this publication will remain unchanged until 2006. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

INTRODUCTION

This part of IEC 60747 should be read in conjunction with IEC 60747-1. It provides basic information on semiconductor

– terminology,
– letter symbols,
– essential ratings and characteristics,
– measuring methods,
– acceptance and reliability.

SEMICONDUCTOR DEVICES –

Part 6: Thyristors

1 Scope

This part of IEC 60747 provides standards for the following categories of discrete semiconductor devices:

– (reverse-blocking) (triode) thyristors,
– asymmetrical (reverse-blocking) (triode) thyristors,
– reverse-conducting (triode) thyristors,
– bidirectional triode thyristors (triacs),
– gate turn-off thyristors (GTO thyristors).

It does not apply to thyristor surge suppressors nor to diacs.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 60747. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this part of IEC 60747 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 60747-1:1983, *Semiconductor devices – Discrete devices and integrated circuits – Part 1: General*

3 Terms and definitions

For the purpose of this part of IEC 60747, the following definitions, together with definitions from IEC 60747-1 and IEC 60050(521), apply.

NOTE 1 For unidirectional thyristors terms and definitions can be written in terms of either “node” and “cathode” or “principal” and “main”. In this standard, the first alternative has been chosen because the second is less suitable for GTO thyristors. In contrast, the second alternative had to be chosen for bidirectional triode thyristors as the first does not apply to them.

NOTE 2 Current and voltage terms and definitions for bidirectional diode thyristors use the adjective “thyristor” because reference to principal current or voltage would imply there is other current or voltage. For the same reason, the adjective “main” is not used with the terminal designations for these devices.

Table 1 summarizes the qualifiers that could be chosen for voltages/currents and terminals.

Table 1 – Qualifiers used for the different kinds of thyristors

Type of thyristor	Triode thyristors	Diode thyristors
Unidirectional thyristors	Anode/cathode voltage/current or principal voltage/current	Anode/cathode voltage/current or thyristor voltage/current
	Anode/cathode terminal or main terminal 1/2	Anode/cathode terminal or terminal 1/2
Bidirectional thyristors	Principal voltage/current	Thyristor voltage/current
	Main terminal 1/2	Terminal 1/2

3.1 Types of thyristors

3.1.1
Classification criteria

Thyristors are classified into subcategories using one or more of the following criteria

a) number of terminals:
   – triode thyristor,
   – diode thyristor;
b) way of acting in the third quadrant of the voltage-current characteristic:
   – unidirectional,
   – bidirectional;
c) physical kind of control:
   – electrically controlled (this usual way of control is not indicated in the term),
   – light-controlled;
d) control capabilities at the gate:
   – only turn on (this restriction is usually not indicated in the term),
   – gate turn-off capability (GTO thyristor);
e) controlled layer:
   – P-gate thyristor (usual technology, not indicated in the term),
   – N-gate thyristor.

3.1.2
thyristor (general)

semiconductor device that is capable, due to internal feedback, of assuming either of two stable states and maintaining the assumed state either with no sustained control current or voltage or at least with considerably less than that necessary to initially establish that state, and that is designed to operate as a switch for the principal or on-state current

NOTE 1 A thyristor is a switch that can be switched on either for only one direction of the principal current (a unidirectional thyristor), or for both directions (a bidirectional thyristor).

NOTE 2 The usual configuration is a PNPN configuration to which can be added other elements needed for additional functions.

NOTE 3 The term “thyristor” may be used for any member of the PNPN family when such use does not result in ambiguity or misunderstanding. In particular, the abbreviated term “thyristor” is widely used for the reverse-blocking triode thyristor, formerly called “semiconductor controlled rectifier”.

3.1.3
unidirectional thyristor
see figure 1

3.1.4
unidirectional triode thyristor
three-terminal thyristor that can switch only when the anode voltage is positive

NOTE In this definition, a second cathode or anode terminal for connecting to the control circuit is not counted.

3.1.5
unidirectional diode thyristor
two-terminal thyristor that can switch only when the anode voltage is positive

3.1.6
bidirectional thyristor
see figure 2

3.1.7
bidirectional triode thyristor (triac)
three-terminal thyristor having substantially the same switching behaviour in the first and third quadrants of the principal characteristic (see curve B of figure 2)

3.1.8
bidirectional diode thyristor
two-terminal thyristor having substantially the same switching behaviour in the first and third quadrants of the thyristor voltage-current characteristic (see curve A of figure 2)

3.1.9
reverse-blocking triode thyristor
unidirectional triode thyristor that exhibits a blocking state in the reverse direction (see curves a) and b) of figure 1)

NOTE If no ambiguity is likely to occur, the term may be abbreviated to “thyristor”.

3.1.10
(symmetrical) reverse-blocking triode thyristor
reverse-blocking triode thyristor whose rated reverse voltage and rated off-state voltage are equal or insignificantly different

3.1.11
asymmetrical reverse-blocking triode thyristor
reverse-blocking triode thyristor whose rated reverse voltage is significantly lower than its rated off-state voltage (see curve b) of figure 1)

3.1.12
reverse-conducting triode thyristor
unidirectional triode thyristor that conducts large currents in the reverse direction at reverse voltages comparable in magnitude to the forward on-state voltage (see curve c) of figure 1)

3.1.13
reverse-blocking diode thyristor
unidirectional diode thyristor that exhibits a blocking state in the reverse direction (see curves a) and b) of figure 1)

3.1.14
(reverse-blocking) gate-turn-off thyristor GTO thyristor
reverse-blocking triode thyristor that can be switched from the on state to the off state as well as from the off state to the on state by applying control signals of appropriate polarity to the gate terminal

3.1.15
reverse-conducting gate-turn-off thyristor
reverse-conducting triode thyristor that can be switched from the on state to the off state as well as from the off state to the on state by applying control signals of appropriate polarity to the gate terminal

3.1.16
symmetrical gate-turn-off thyristor
gate-turn-off thyristor whose rated reverse voltage and rated off-state voltage are equal or insignificantly different

3.1.17
asymmetrical gate-turn-off thyristor
gate-turn-off thyristor whose rated reverse voltage is significantly lower than its rated off-state voltage

3.1.18
P-gate thyristor
unidirectional triode thyristor whose gate terminal is connected to the P region nearest the cathode and that is normally switched to the on state by applying a positive signal to the gate terminal with respect to the cathode terminal

3.1.19
N-gate thyristor
unidirectional triode thyristor whose gate terminal is connected to the N region nearest the anode and that is normally switched to the on state by applying a negative signal to the gate terminal with respect to the anode terminal

NOTE Any practical realization of an N-gate thyristor was not known when this publication was issued.

3.2 Basic terms defining the static voltage-current characteristics of triode thyristors

3.2.1
gate terminal
terminal unique to the control circuit

3.2.2
gate current
(control) current into the gate terminal

3.2.3
principal current
current that is switched (controlled) by the thyristor

3.2.4
main terminals
two terminals through which the principal current flows

3.2.5
anode terminal (of a unidirectional triode thyristor)
main terminal to which the principal current flows from the circuit being controlled when the thyristor is in the on state

NOTE A second anode terminal may be provided for connecting to the control circuit of an N-gate thyristor.

3.2.6
cathode terminal (of a unidirectional triode thyristor)
main terminal from which the principal current flows to the circuit being controlled when the thyristor is in the on state

NOTE A second cathode terminal may be provided for connecting to the control circuit of a P-gate thyristor.

3.2.7
main terminal 1 (of a bidirectional triode thyristor (triac)) (MT1)
main terminal intended by the triac manufacturer to conduct the control current in addition to the principal current

NOTE Some bidirectional triode thyristors are completely symmetrical, e.g. Silicon Bilateral Switch (SBS) thyristors. For these, the choice for the manufacturer is arbitrary, and the user can return the control circuit to whichever main terminal will provide the required polarity of gate current.

3.2.8
main terminal 2 (of a bidirectional triode thyristor (triac)) (MT2)
other main terminal after main terminal 1 has been designated by the triac manufacturer

3.2.9
anode-cathode voltage
anode voltage (of an unidirectional triode thyristor)
voltage (potential difference) between anode and cathode terminals

3.2.10
principal voltage
voltage (potential difference) between the main terminals

NOTE 1 In the case of unidirectional triode thyristors, the principal voltage is called positive when the anode potential is more positive than the cathode potential and called negative when the anode potential is less positive than the cathode potential. Thus, for these thyristors, “principal voltage” and “anode-cathode voltage” are synonymous.

NOTE 2 In the case of bidirectional triode thyristors, the polarity of the principal voltage (with regard to main terminals 1 and 2) is to be specified.

3.2.11
(static) voltage-current characteristic
(static) principal characteristic (of a unidirectional triode thyristor (see figure 1))
function, usually represented graphically, relating the anode voltage to the anode current for a specified virtual junction temperature, under conditions of internal electrical and thermal equilibrium

NOTE 1 Where applicable, the characteristic may be given with the gate current as a parameter.

NOTE 2 The word “static” is usually omitted except when a distinction between static and dynamic characteristics is necessary.

3.2.12
(static) principal characteristic (of a bidirectional triode thyristor (see figure 2))
function, usually represented graphically, relating the principal voltage to the principal current for a specified virtual junction temperature, under conditions of internal electrical and thermal equilibrium

NOTE 1 Where applicable, the characteristic may be given with the gate current as a parameter.

NOTE 2 The word “static” is usually omitted except when a distinction between static and dynamic characteristics is necessary.

3.3 Basic terms defining the static voltage-current characteristics of diode thyristors

3.3.1
anode terminal (of a unidirectional diode thyristor)
terminal to which the current flows from the external circuit when the thyristor is in the on state

3.3.2
cathode terminal (of a unidirectional diode thyristor)
terminal from which the current flows to the external circuit when the thyristor is in the on state

3.3.3
terminal 1 (of a bidirectional diode thyristor)
terminal that is designated “1” by the manufacturer

3.3.4
terminal 2 (of a bidirectional diode thyristor)
terminal that is designated “2” by the manufacturer

3.3.5
anode-cathode voltage
anode voltage(of a unidirectional diode thyristor)
voltage between the anode and cathode terminals

NOTE The anode-cathode voltage is called positive when the anode potential is higher than the cathode potential, and called negative when the anode potential is lower than the cathode potential.

3.3.6
thyristor voltage (of a bidirectional diode thyristor)
voltage between the two terminals

NOTE The polarity of the thyristor voltage (with regard to terminals 1 and 2) is to be specified.

3.3.7
(static) characteristic (of a unidirectional diode thyristor)
function, usually represented graphically, relating the anode voltage to the anode current for a specified virtual junction temperature, under conditions of internal electrical and thermal equilibrium

NOTE The word “static” is usually omitted, except when a distinction between static and dynamic characteristics is necessary.

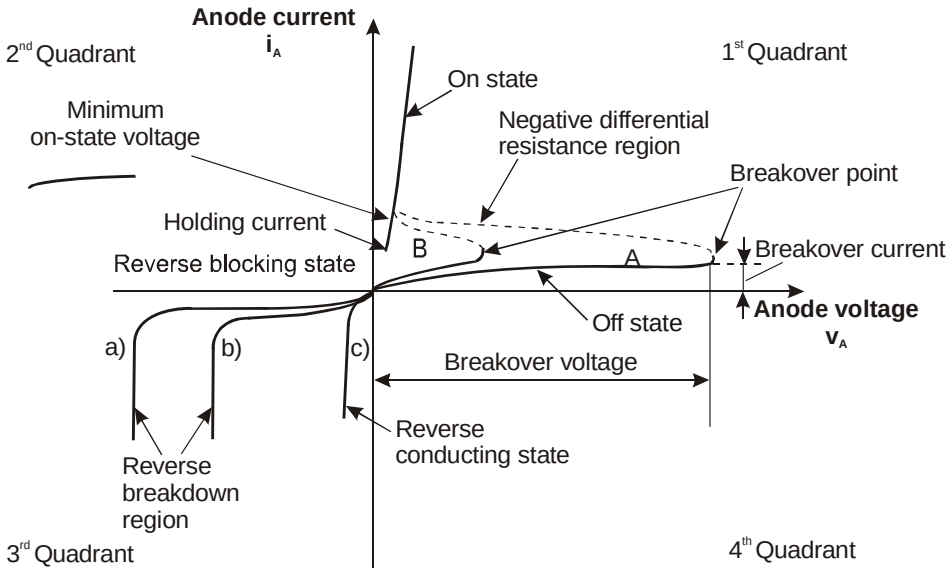
3.3.8
(static) characteristic (of a bidirectional diode thyristor)
function, usually represented graphically, relating the thyristor voltage to the thyristor current for a specified virtual junction temperature, under conditions of internal electrical and thermal equilibrium

NOTE The word “static” is usually omitted, except when a distinction between static and dynamic characteristics is necessary.

3.4 Particulars of the static voltage-current characteristics of triode and diode thyristors (see figures 1 and 2)

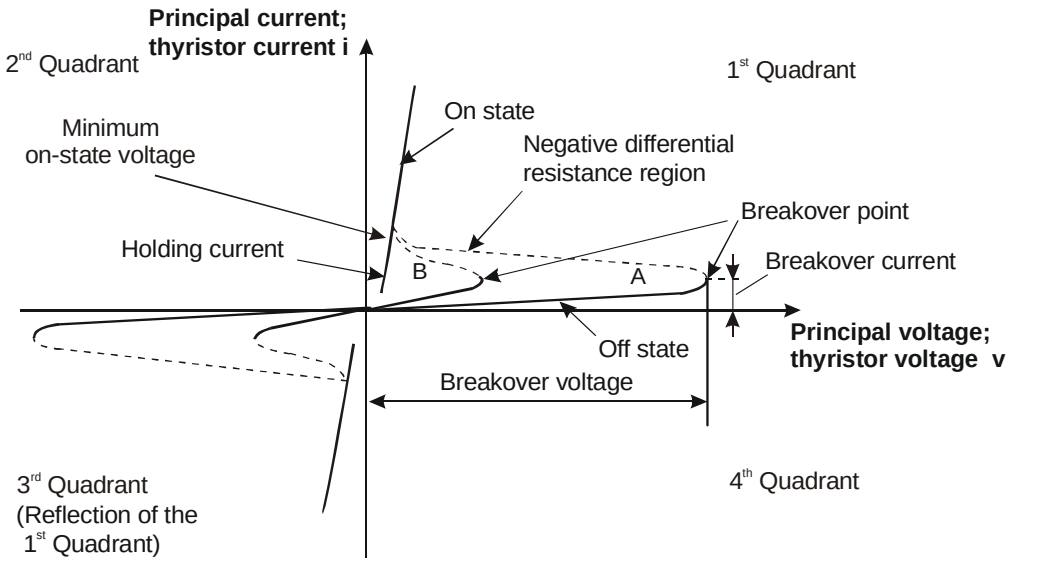
NOTE The states referred to in 3.4.2 through 3.4.7 concern portions of the static characteristic, i.e. static states, although in the more general terms, this restriction is not indicated. If necessary, distinction will be made between static and dynamic states.

3.4.1
on state
state of a thyristor, in a quadrant in which switching may occur, that corresponds to the low-resistance portion of the characteristic



Curve A zero gate current
Curve B gate current greater than zero
Curve a) reverse-blocking thyristor
Curve b) asymmetrical thyristor
Curve c) reverse-conducting thyristor

Figure 1 – Particulars of the static characteristic of unidirectional thyristors



Curve A bidirectional diode thyristors or bidirectional triode thyristors with zero gate current
Curve B bidirectional triode thyristors with gate current greater than zero

Figure 2 – Particulars of the static characteristic of bidirectional thyristors

3.4.2
off state
state of a thyristor, in a quadrant in which switching may occur, that corresponds to the portion of the characteristic between the origin and the breakover point

3.4.3
reverse-blocking state
state of a reverse-blocking or asymmetrical thyristor that corresponds to a reverse voltage between the origin and the beginning of the reverse breakdown region

3.4.4
reverse breakdown region
portion of the characteristic in which reverse breakdown occurs (the term “reverse breakdown” is defined in IEC 60747-1)

3.4.5
reverse-conducting state
state of a reverse-conducting triode thyristor that corresponds to the third quadrant of the characteristic

3.4.6
negative differential resistance region
any portion of the characteristic within which the differential resistance is negative

3.4.7
breakover point
in a quadrant in which switching may occur, the point for which the differential resistance is zero and the off-state voltage reaches a maximum value

3.5 Terms related to ratings and characteristics; principal voltages

NOTE 1 In this subclause, similar definitions for more than one kind of thyristor are combined in a single wording in which reference is made to all relevant qualifiers. For example, in 3.5.8, the wording “anode, principal, or thyristor voltage” indicates that the term “on-state voltage” applies to unidirectional thyristors, bidirectional triode thyristors and bidirectional diode thyristors (see table 1).

NOTE 2 When several distinctive forms of letter symbols exist, the most commonly used form(s) is (are) given.

3.5.1
breakover voltage ($V_{(BO)}$)
voltage at the breakover point

3.5.2
reverse voltage (of a unidirectional thyristor) (V_R)
negative anode voltage

3.5.3
direct reverse voltage (of a unidirectional thyristor) ($V_{R(D)}$)
reverse voltage that is independent of time or in which the changes are so small that they can be neglected

3.5.4
reverse breakdown voltage (of a unidirectional thyristor) ($V_{(BR)}$)
voltage in the reverse breakdown region

3.5.5
crest working reverse voltage
peak working reverse voltage (of a unidirectional thyristor) (V_{RWM})

highest instantaneous value of the reverse voltage, excluding all repetitive and non-repetitive transient voltages (see figure 3)

NOTE The repetitive voltage is usually a function of the circuit and increases the power loss of the device. A non-repetitive transient voltage is usually due to an external cause, and it is assumed that its effect has completely disappeared before the next transient arrives.

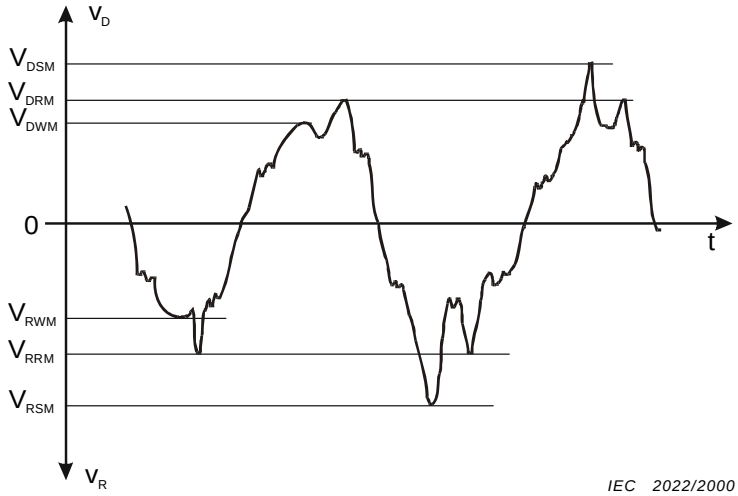


Figure 3 – Peak reverse and peak off-state voltages of a thyristor

3.5.6
repetitive peak reverse voltage (of a unidirectional thyristor) (V_{RRM})
highest instantaneous value of the reverse voltage, including all repetitive transient voltages, but excluding all non-repetitive transient voltages (see figure 3)

NOTE The repetitive voltage is usually a function of the circuit and increases the power loss of the device. A non-repetitive transient voltage is usually due to an external cause, and it is assumed that its effect has completely disappeared before the next transient arrives.

3.5.7
non-repetitive peak reverse voltage;
peak transient reverse voltage (of a unidirectional thyristor) (V_{RSM})

highest instantaneous value of any non-repetitive transient reverse voltage (see figure 3)

NOTE See note to 3.5.5. (The repetitive voltage is usually a function of the circuit and increases the power loss of the device. A non-repetitive transient voltage is usually due to an external cause, and it is assumed that its effect has completely disappeared before the next transient arrives.)

NOTE 2 Preference should be given to the term “non-repetitive peak reverse voltage”.

3.5.8
on-state voltage (V_T)
anode, principal, or thyristor voltage when the thyristor is in the on state

3.5.9
off-state voltage (V_D)
anode, principal, or thyristor voltage when the thyristor is in the off state

3.5.10
direct off-state voltage ($V_{D(D)}$)
off-state voltage that is independent of time or in which the changes are so small that they can be neglected

3.5.11
crest working off-state voltage
peak working off-state voltage (V_{DWM})
highest instantaneous value of the off-state voltage, excluding all repetitive and non-repetitive transient voltages (see figure 3)

NOTE The repetitive voltage is usually a function of the circuit and increases the power loss of the device. A non-repetitive transient voltage is usually due to an external cause, and it is assumed that its effect has completely disappeared before the next transient arrives.

3.5.12
repetitive peak off-state voltage (V_{DRM})
highest instantaneous value of the off-state voltage, including all repetitive transient voltages, but excluding all non-repetitive transient voltages (see figure 3)

NOTE The repetitive voltage is usually a function of the circuit and increases the power loss of the device. A non-repetitive transient voltage is usually due to an external cause, and it is assumed that its effect has completely disappeared before the next transient arrives.

3.5.13
non-repetitive peak off-state voltage
peak transient off-state voltage (V_{DSM})
highest instantaneous value of any non-repetitive transient off-state voltage (see figure 3)

NOTE 1 The repetitive voltage is usually a function of the circuit and increases the power loss of the device. A non-repetitive transient voltage is usually due to an external cause, and it is assumed that its effect has completely disappeared before the next transient arrives

NOTE 2 Preference should be given to the term “non-repetitive peak off-state voltage”

3.5.14
critical rate of rise of off-state voltage ($(dv_D/dt)_{cr}$)
highest value of the rate of rise of off-state voltage that will note cause switching from the off state to the on state.

NOTE 1 The measuring method for the rate of rise is to be specified.

NOTE 2 If no ambiguity is likely to result, the shorter expression “dv/dt” may be used.

3.5.15
critical rate of rise of commutating voltage (of a reverse-conducting triode thyristor) ($(dv_{D(com)}/dt)_{cr}$)
highest value of the rate of rise of off-state voltage, immediately following reverse current conduction, that will not cause switching from the off state to the on state

NOTE 1 The measuring method for the rate of rise is to be specified.

NOTE 2 If no ambiguity is likely to result, the shorter expression “$dv_{(com)}/dt$” may be used.

3.5.16
critical rate of rise of commutating voltage
critical rate of rise of the reapplied off-state voltage (of a triac) ($(dv_{D(com)}/dt)_{cr}$)
highest value of the rate of rise of off-state voltage, immediately following on-state current conduction in the opposite direction, that will not cause switching from the off state to the on state

NOTE 1 The measuring method for the rate of rise is to be specified.

NOTE 2 If ambiguity is likely to result, the shorter expression “$dv_{(com)}/dt$” may be used.

3.5.17
turn-off (off-state) spike voltage (of a GTO thyristor) ($V_{Q(SP)}$)
peak value of a spike on the reapplied off-state voltage that occurs shortly after the off-state voltage begins to rise (see figure 13)

NOTE The turn-off spike voltage is not an inherent characteristic of the thyristor as its value depends on the parasitic inductance in the snubber network connected in parallel to the GTO thyristor. Its value has an influence on the turn-off energy loss.

3.5.18
turn-off peak off-state voltage (of a GTO thyristor) (V_{DQM})
peak value, higher than the final steady-state value, to which the re-applied off-state voltage rises towards the end of the turn-off process (see figure 13)

NOTE The turn-off peak off-state voltage is not an inherent characteristic of the GTO thyristor as its value depends on the design of the external circuits. Its value has an influence on the turn-off energy loss.

3.6 Terms related to ratings and characteristics; principal currents

3.6.1
breakover current ($I_{(BO)}$)
anode, principal, or thyristor current at the breakover point

3.6.2
reverse current (of a unidirectional thyristor) (I_R)
anode current for a negative anode voltage

3.6.3
reverse-conducting current (of a reverse-conducting thyristor) (I_{RC})
reverse current of a reverse-conducting thyristor

3.6.4
mean reverse-conducting current ($I_{RC(AV)}$)
value of the reverse-conducting current averaged over a full cycle

3.6.5
overload reverse-conducting current ($I_{RC(OV)}$)
reverse-conducting current whose continuous application would cause the maximum rated virtual junction temperature to be exceeded, but that is limited in duration such that this temperature is not exceeded

NOTE 1 Devices may be subjected to overload currents as frequently as called for by the application, while being subjected to normal operating voltages.

NOTE 2 If not otherwise stated, specifications for the rated (limiting) value of an overload reverse-conducting current refer to a waveshape hat is substantially the same as for the rated value of the reverse-conducting current.

3.6.6
surge reverse-conducting current (I_{RCSM})
reverse-conducting current pulse of short duration and specified waveshape, whose application causes or would cause the maximum rated virtual junction temperature to be exceeded, but which is assumed to occur rarely and with a limited number of such occurrences during the service life of the device and to be a consequence of unusual circuit conditions (for example, a fault)

3.6.7
reverse blocking current (of a unidirectional thyristor) (I_R)
reverse current when a thyristor is in the reverse-blocking state

3.6.8
reverse recovery current (of a unidirectional thyristor) (I_{RR}, $I_{R(REC)}$)
reverse current that occurs during the reverse recovery time

NOTE For the peak value of the reverse recovery current during the reverse recovery time, only the letter symbol I_{RM} or $I_{RM(REC)}$ may be used (see figure 9) because the letter symbol I_{RRM} is already attributed to the repetitive peak reverse current.

3.6.9
on-state current (I_T)
anode, principal, or thyristor current when the thyristor is in the on state

3.6.10
direct on-state current ($I_{T(D)}$)
on-state current that is independent of time or in which the changes are so small that they can be neglected

3.6.11
mean on-state current ($I_{T(AV)}$)
value of the on-state current averaged over a full cycle

3.6.12
r.m.s. on-state current ($I_{T(RMS)}$)
r.m.s. value of the on-state current averaged over a full cycle

3.6.13
peak sinusoidal on-state current (I_{TM})
peak value of a sinusoidal on-state current, excluding any transient currents

3.6.14
peak trapezoidal on-state current (I_{TM})
peak value of a trapezoidal on-state current, excluding any transient currents

3.6.15
repetitive peak on-state current (I_{TRM})
peak value of the on-state current, including all repetitive transient currents (see figure 4)

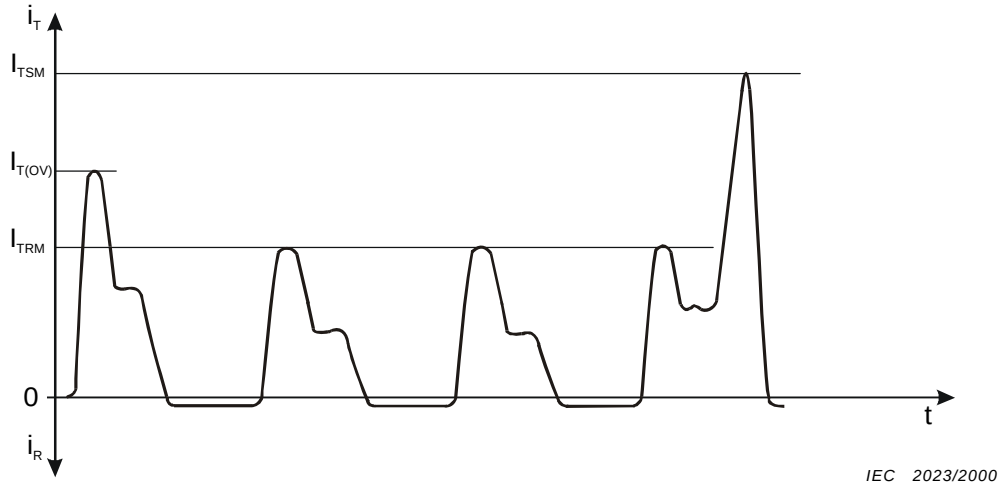


Figure 4 – Peak values of on-state currents

3.6.16
overload on-state current ($I_{T(OV)}$)
on-state current whose continuous application would cause the maximum-rated virtual junction temperature to be exceeded, but that is limited in duration such that this temperature is not exceeded (see figure 4)

NOTE 1 Devices may be subjected to overload currents as frequently as called for by the application while being subjected to normal operating voltages.

NOTE 2 If not otherwise stated, specifications for the rated (limiting) value of an overload on-state current refer to a waveshape that is substantially the same as for the rated value of the on-state current.

3.6.17
surge on-state current (I_{TSM})
on-state current pulse of short duration and specified waveshape, whose application causes or would cause the maximum rated virtual junction temperature to be exceeded, but which is assumed to occur rarely and with a limited number of such occurrences during the service life of the device and to be a consequence of unusual circuit conditions (for example, a fault) (see figure 4)

3.6.18
I^2t value (of a surge on-state current) (I^2t)
value used for the specification of a maximum rated value of surge on-state current, given in terms of the maximum rated value of

$$I^2 t = \int_0^{t_i} i^2 dt$$

for a specified short integration time t_i

3.6.19
repetitive peak controllable on-state current (of a GTO thyristor) (I_{TQRM})
highest peak value of the on-state current that can be turned off periodically by means of gate control

NOTE A repetitive current is usually a function of the circuit and increases the power loss within the device. A non-repetitive transient current is usually due to an external cause and it is assumed that its effect has completely disappeared before the next transient arrives.

3.6.20
non-repetitive peak controllable on-state current (of a GTO thyristor) (I_{TQSM})
highest non-repetitive peak value of the on-state current that can be turned off by means of gate control

NOTE A repetitive current is usually a function of the circuit and increases the power loss within the device. A non-repetitive transient current is usually due to an external cause and it is assumed that its effect has completely disappeared before the next transient arrives.

3.6.21
peak case non-rupture current (I_{RSMC})
peak value of reverse current that should not be exceeded in order to avoid bursting of the case or the emission of a plasma beam, under specified conditions of the waveshape and duration of the reverse current pulse

NOTE 1 This definition implies that a fine crack in the case is tolerated, if found in a device subjected to the peak case non-rupture current, provided that no plasma beam was emitted, parts of the case did not break away, and the device did not melt externally or burst into flames.

NOTE 2 Such very high reverse currents may occur in large thyristor assemblies if one of the thyristors has a reverse breakdown. Very large thyristors may have a peak surge on-state current that is higher than the peak case non-rupture current so that a fuse selected for the peak surge on-state current cannot provide protection against rupture of the case.

3.6.22
case non-rupture I^2 t value (I_{RSC}^2 t)
value of I_{RSC}^2 t that should not be exceeded in order to avoid bursting of the case or the emission of a plasma beam, under specified conditions of the waveshape and duration of the reverse current pulse and given as follows:

$$I_{RSC}{}^2 t = \int_0^{t_p} i_R{}^2 \ dt$$

where t_p is the reverse current pulse duration

NOTE 1 This definition implies that a fine crack in the case is tolerated if found in a device subjected to the case non-rupture I^2t value, provided that no plasma beam was emitted, parts of the case did not break away, and the device did not melt externally or burst into flames.

NOTE 2 Such very high reverse currents may occur in large thyristor assemblies if one of the thyristors has a reverse breakdown. Very large thyristors may have an (on-state) I^2t value that is higher than the case non-rupture $I_{RSC}{}^2t$ value so that a fuse selected for the I^2t value cannot provide protection against rupture of the case.

3.6.23
critical rate of rise of on-state current ($(di_T/dt)_{cr}$)
highest value of the rate of rise of on-state current that a thyristor can withstand without deleterious effect

3.6.24
latching current (I_L)
minimum anode or principal current required to maintain the thyristor in the on-state immediately after the triggering condition has been removed following switching from the off state to the on state

3.6.25
holding current (I_H)
minimum anode, principal, or thyristor current that will maintain the thyristor in the on state

3.6.26
off-state current (I_D)
anode, principal, or thyristor current when the thyristor is in the off state

3.6.27
direct off-state current ($I_{D(D)}$)
off-state current that is independent of time or in which the changes are so small that they can be neglected

3.6.28
tail current (of a GTO thyristor) (I_Z)
anode current that flows during the tail time (see figure 13)

3.6.29
peak tail current (of a GTO thyristor) (I_{ZM})
peak value of tail current that occurs shortly after the beginning of the tail time (see figure 13)

3.7 Terms related to ratings and characteristics; gate voltages and currents

3.7.1
gate voltage (V_G)
voltage between the gate terminal and

- for unidirectional triode thyristors, the cathode in the case of a P-gate thyristor and the anode in the case of an N-gate thyristor,
- for bidirectional triode thyristors, the specified main terminal

3.7.2
gate current (I_G)
(control) current into the gate terminal

3.7.3
forward gate voltage (V_{FG})
– for P-gate thyristors, the positive gate-cathode voltage
– for N-gate thyristors, the negative gate-anode voltage

3.7.4
peak forward gate voltage (V_{FGM})
highest instantaneous value of the forward gate voltage including all transient voltages

3.7.5
reverse gate voltage (V_{RG})
– for P-gate thyristors, the negative gate-cathode voltage
– for N-gate thyristors, the positive gate-anode voltage

3.7.6
peak reverse gate voltage (V_{RGM})
highest instantaneous value of the reverse gate voltage including all transient voltages

3.7.7
forward gate current (I_{FG})
– for P-gate thyristors, the positive gate current
– for N-gate thyristors, the negative gate current

3.7.8
peak forward gate current (I_{FGM})
highest instantaneous value of the forward gate current including all transient currents

3.7.9
reverse gate current (I_{RG})
– for P-gate thyristors, the negative gate current
– for N-gate thyristors, the positive gate current

3.7.10
peak reverse gate current (I_{RGM})
highest instantaneous value of the reverse gate current including all transient currents

3.7.11
sustaining gate current (of a GTO thyristor) (I_{FGsus})
minimum forward gate current required to ensure that, if the anode current drops below the value required to keep all the subdivided cathode areas in conduction, they will all return to conduction when the anode current is increased again

3.7.12
turn-on gate voltage (v_{FGT})
forward gate voltage during the time interval within which the thyristor is turning on

3.7.13
turn-on gate drive voltage (V_{FGT})
gate voltage required to produce the turn-on gate drive current

3.7.14
on-state gate bias voltage (V_{FGB})
forward gate voltage during the time interval following the time within which the thyristor was turning on

3.7.15
turn-off gate voltage (of a GTO thyristor) (V_{RGQ})
reverse gate voltage during the time interval within which the thyristor is turning off

3.7.16
peak turn-off gate voltage (of a GTO thyristor) (V_{RGQM})
peak value of the turn-off gate voltage at the end of its rapid rise after the peak value of turn-off gate current (I_{RGQM}) has been reached

3.7.17
turn-off gate bias voltage (of a GTO thyristor) (V_{RGQB})
essentially constant value of the turn-off gate voltage that occurs towards the end of the turn-off process, in the case where the gate-control circuit supports this process by maintaining the turn-off gate voltage at a value that is higher than the off-state gate bias voltage

3.7.18
off-state gate bias voltage (of a GTO thyristor) (V_{RGB})
reverse gate voltage during the time interval following the time within which the thyristor was turning off

3.7.19
turn-on gate current (i_{FGT})
forward gate current during the time interval within which the thyristor is turning on

3.7.20
turn-on gate drive current (I_{FGT})
turn-on gate current supplied by the trigger circuit

NOTE Often the turn-on process is accelerated by an extra high peak current at the beginning of the trigger pulse (see figure 12).

3.7.21
peak turn-on gate drive current (I_{FGTM})
peak value of the turn-on gate drive current pulse

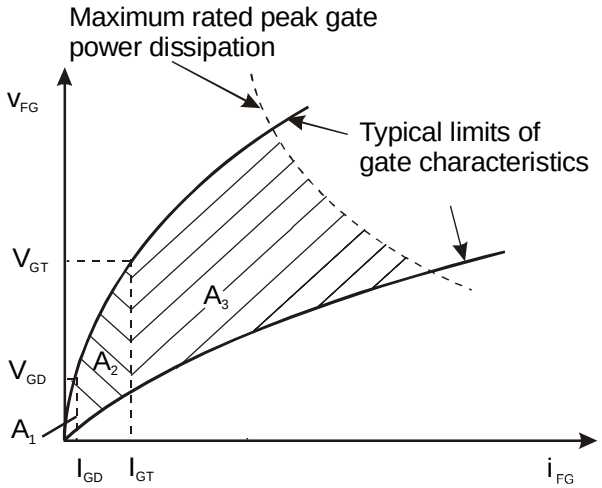
3.7.22
on-state gate bias current (I_{FGB})
forward gate current during the time interval following the time within which thyristor was turning on

3.7.23
turn-off gate current (of a GTO thyristor) (I_{RGQ})
reverse gate current during the time interval within which thyristor is turning off

3.7.24
turn-off gate bias current (of a GTO thyristor) (I_{RGQB})
gate current associated with the turn-off gate bias voltage V_{RGQB}

3.7.25
peak turn-off gate current (of a GTO thyristor) (I_{RGQM})
peak value of the reverse gate current reached at the end of its rapid rise in the beginning of the turn-off process

NOTE Specifications refer to the minimum value of I_{RGQM} that the gate turn-off pulse generator is capable of supplying as a function of the peak on-state current to be switched off under specified conditions.



A_1, A_2, A_3 see figure 20.

Figure 5 – Forward gate voltage versus forward gate current

3.7.26
off-state gate bias current (I_{RGB})
reverse gate current during the time interval following the time within which the thyristor was turned off

3.7.27
gate trigger current (I_{GT})
lowest gate current required to safely trigger any thyristor of a type under specified conditions

3.7.28
gate trigger voltage (V_{GT})
gate voltage required to produce the gate trigger current

3.7.29
gate non-trigger current (I_{GD})
highest value of an undesired current in the gate circuit which will safely not trigger any thyristor which is under specified conditions

3.7.30
gate non-trigger voltage (V_{GD})
gate voltage associated with the gate non-trigger current

3.8 Terms related to ratings and characteristics; powers, energies and losses

NOTE 1 All definitions are written in terms of triode thyristors. Where appropriate, they apply also to diode thyristors.

NOTE 2 All definitions for power, energy and losses refer, if not otherwise specified, to the product of anode or principal current and anode or principal voltage.

A Instantaneous power during a cycle

NOTE 1 The following definitions refer to a chronological subdivision of the cycle time into particular intervals during which the thyristor is either in a particular state or during which it changes state.

NOTE 2 The definitions are general. They do not consider that the beginning and ending of the particular time interval should be identified in order to make specifications for the derived characteristics “mean partial power loss” and “partial energy loss” meaningful. However, guidance for the specification of these times is given in the relevant notes.

3.8.1
reverse power (P_R)
power when the thyristor is in the reverse-blocking state

NOTE If not otherwise specified, the term refers to the power in the time interval between the ending of the turn-off time and the change from the reverse blocking state to the off state (either I = 0 or V = 0).

3.8.2
reverse-conducting power (of a reverse-conducting thyristor) (P_{RC})
power while the thyristor is in the reverse-conducting state

NOTE If not otherwise specified, the term refers to the power in the time interval between the ending of the turn-off time and the change from the reverse conducting state to the off state (either I = 0 or V = 0).

3.8.3
off-state power (P_D)
power while the thyristor is in the off state

NOTE If not otherwise specified, the term refers to the power generated during the time interval between the crossing of the origin from the reverse blocking (or conducting) state to the off state (I = 0 or V = 0) and the beginning of the turn-on time, with GTO thyristors; in addition during the time interval between the ending of the turn-off time and the crossing of the origin from the off state to the reverse-blocking (or conducting) state.

3.8.4
turn-on power (P_{TT})
power in the time interval during which the thyristor is turning on

NOTE If not otherwise specified, this time interval corresponds with the turn-on time.

3.8.5
on-state power (P_T)
power while the thyristor is in the on state

NOTE If not otherwise specified, the term refers to the power during the period between the ending of the turn-on time and the beginning of the turn-off time.

3.8.6
turn-off power (P_{RQ}); for GTO thyristors: (P_{DQ})
power in the time interval during which the thyristor is turning off

NOTE If not otherwise specified, this time interval corresponds with the turn-off time.

3.8.7
gate power (P_G)
product of the instantaneous values of gate current and voltage

B Mean power losses

NOTE 1 The term “power dissipation” has been used in the past as a true synonym for “power loss”. This is no longer recommended. The term “loss” should refer to the loss at the place of its origin and the term “dissipation” should refer to the heat that is dissipated from the surface of the device into the environment. Different terms are provided for the two quantities because, due to internal storage of heat, the two differ with time.

NOTE 2 As an exception, “mean power dissipation” may still be used as a synonym for “mean power loss”, but only where appropriate, i.e. when the different course with time has no influence on the mean values of the two. This is the case when the mean values are averaged over a full cycle.

3.8.8
mean partial power loss
mean value of the instantaneous power loss in a particular time interval of the cycle, averaged over the full cycle

3.8.9
mean total power loss ($P_{tot(AV)}$)
sum of all mean partial power losses and the mean gate power loss, during a full cycle

$$P_{tot(AV)} = P_{T(AV)} + P_{add(AV)} + P_{G(AV)}$$

3.8.10
mean on-state power loss ($P_{T(AV)}$)
mean partial power loss resulting from on-state power

3.8.11
mean additional power loss ($P_{add(AV)}$)
Sum of $P_{add(AV)} = P_{TT(AV)} + P_{RQ(AV)} + P_{D(AV)} + P_{R(AV)}$
With GTO thyristors, $P_{RQ(AV)}$ is replaced by $P_{DQ(AV)}$.

3.8.12
mean turn-on power loss ($P_{TT(AV)}$)
mean partial power loss resulting from the turn-on power

3.8.13
mean turn-off power loss ($P_{RQ(AV)}$); for GTO thyristors: ($P_{DQ(AV)}$)
mean partial power loss resulting from turn-off power

3.8.14
mean off-state power loss ($P_{D(AV)}$)
mean partial power loss resulting from off-state power

3.8.15
mean reverse power loss ($P_{R(AV)}$)
mean partial power loss resulting from reverse power

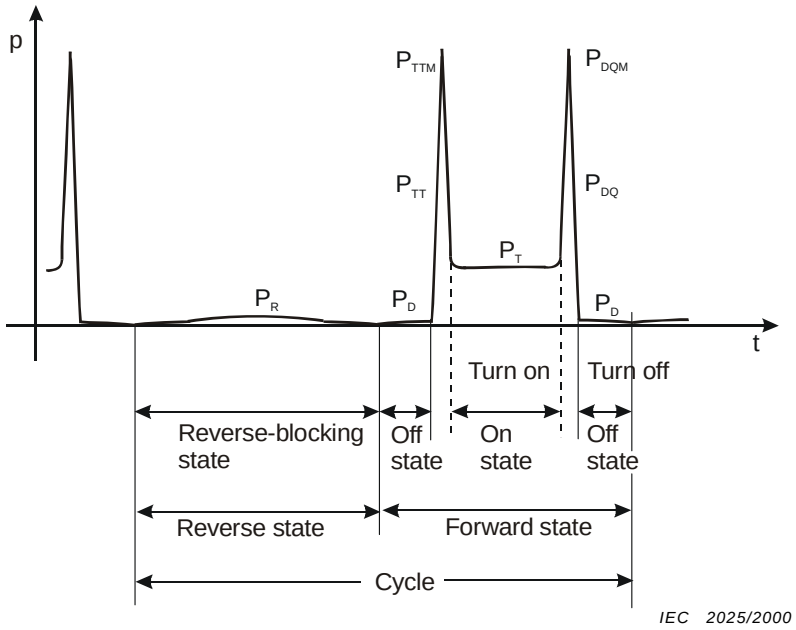
3.8.16
mean gate power loss ($P_{G(AV)}$)
gate power loss averaged over a full cycle

C Energy losses (for GTO thyristors: see figure 7)

3.8.17
dynamic on-state energy loss (E_T)
total energy loss from the instant when the rising on-state current reaches a specified low value to the instant that defines the beginning of the turn-off time

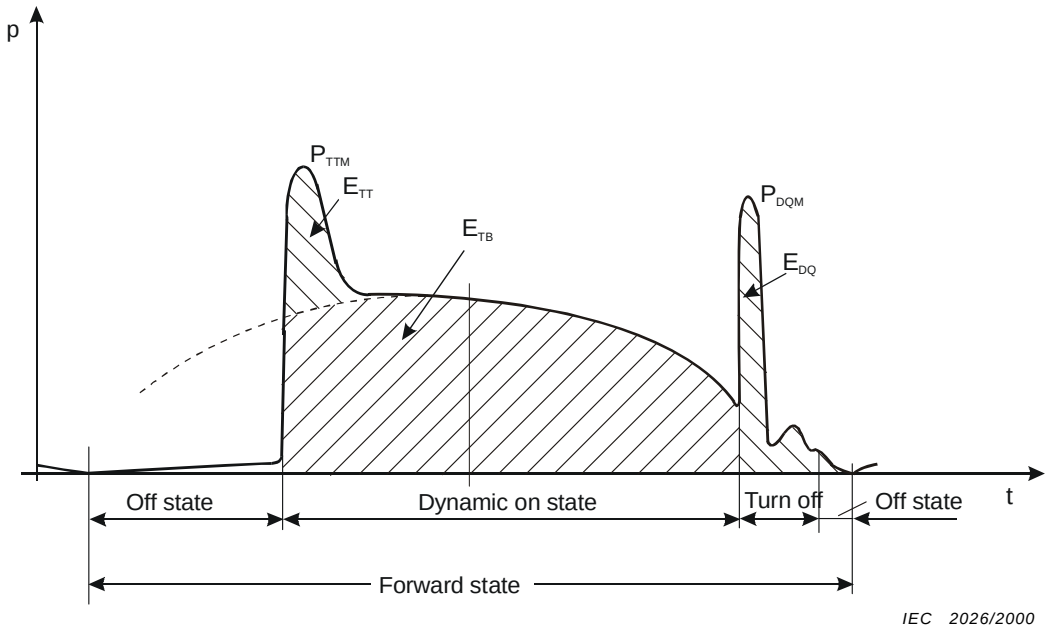
3.8.18
basic on-state energy loss (E_{TB})
energy loss that would result from the flow of on-state current if the thyristor were fully turned on during the entire on-state period

NOTE This energy loss can only be determined by calculations based on the observed waveform of the current. The calculation method is to be specified.



P_R reverse power
P_D off-state power
P_T on-state power
P_{TT} turn-on power
P_{DQ} turn-off power

Figure 6 – Partial power (losses) of GTO thyristors at relatively low frequencies



E_{TB} basic on-state energy loss
E_{TT} additional turn-on energy loss
$E_T = E_{TB} + E_{TT}$ dynamic (total) on-state energy loss
E_{DQ} turn-off energy loss

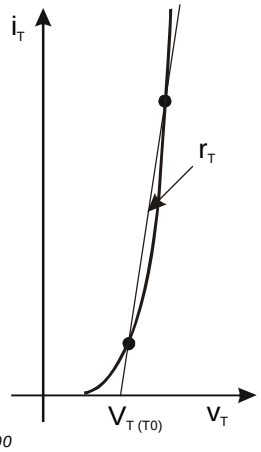
Figure 7 – Components of dynamic on-state energy loss of GTO thyristors at relatively high frequencies

3.8.19
additional turn-on energy loss (E_{TT})
calculated difference between the dynamic on-state energy loss and the basic on-state energy loss:

$$E_{TT} = E_T - E_{TB}$$

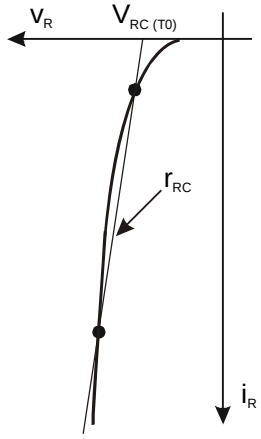
3.8.20
turn-off energy loss (E_{RQ}); for GTO thyristors: (E_{DQ})
energy loss during the turn-off time

3.9 Terms related to ratings and characteristics; recovery times and other characteristics



IEC 2027/2000

Figure 8a – On-state characteristic



IEC 2028/2000

Figure 8b – Reverse-conducting characteristic

Figure 8 – Approximation of characteristics

A Approximation of the on-state characteristic (see figure 8a)

3.9.1
straight-line approximation of the on-state characteristic
approximation of the current versus voltage on-state characteristic by means of a straight line that crosses this characteristic at two specified points

3.9.2
on-state slope resistance (r_T)
value of the resistance calculated from the slope of the straight-line approximation of the on-state characteristic

3.9.3
on-state threshold voltage ($V_{T(TO)}$, $V_{(TO)}$)
value of the on-state voltage obtained at the intersection of its straight-line approximation with the voltage axis

B Approximation of the reverse-conducting characteristic (see figure 8b)

3.9.4
straight-line approximation of the reverse-conducting characteristic
approximation of the current versus voltage reverse-conducting characteristic by means of a straight line that crosses this characteristic at two specified points

3.9.5
reverse-conducting slope resistance (r_{RC})
value of the resistance calculated from the slope of the straight-line approximation of the reverse-conducting characteristic

3.9.6
reverse-conducting threshold voltage ($V_{RC(TO)}$)
value of the reverse voltage obtained at the intersection of its straight-line approximation with the voltage axis

C Thermal characteristics, basic definitions

The definitions given in IEC 60747-1, chapter IV, apply. The following additional definitions may be useful.

D Partial thermal resistances (of thyristors in disc-type housings)

3.9.7
partial thermal resistance junction-to-case, anode side ($R_{th(j-c)A}$)
thermal resistance between the virtual junction and the anode side of the case

3.9.8
partial thermal resistance junction-to-case, cathode side ($R_{th(j-c)K}$)
thermal resistance between the virtual junction and the cathode side of the case

E Partial thermal resistances (of reverse-conducting thyristors with integrated inverse diodes)

NOTE 1 As on-state power loss and reverse-conducting power loss occur in different places, a distinction between the thyristor junction-to-case thermal resistance and the diode junction-to-case thermal resistance may be necessary.

NOTE 2 The application of specifications for these partial thermal resistance's in the case of concurrent power losses in the thyristor and in the reverse diode is under consideration.

3.9.9
thyristor junction-to-case thermal resistance ($R_{th(j-c)T}$)
quotient of

– the temperature difference between the thyristor junction and the reference point, by

– the steady-state on-state power loss in the thyristor, under the condition that the whole power loss in the device is due to on-state current.

3.9.10
diode junction-to-case thermal resistance ($R_{th(j-c)D}$)
quotient of

– the temperature difference between the diode junction and the reference point, by

– the steady-state reverse conducting power loss in the diode, under the condition that the whole power loss in the device is due to reverse-conducting current

F Recovery times

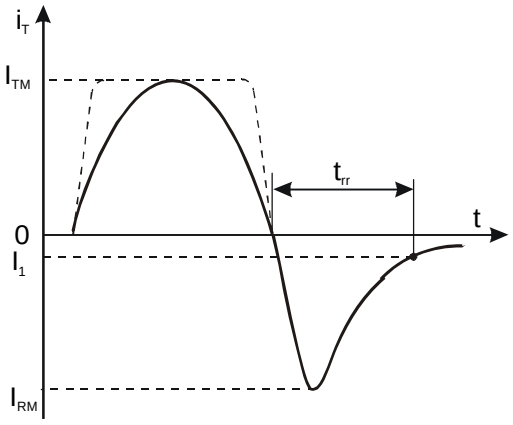
3.9.11
reverse recovery time (of a reverse-blocking thyristor) (t_{rr})
time interval between

– the instant when the current passes through zero while changing from the on state to the reverse-blocking state, and

– the instant when either the reverse current is reduced from its peak value I_{RM} to a specified low value (as shown in figure 9a and which may be zero), or the extrapolated reverse current reaches zero (as shown in figure 9b).

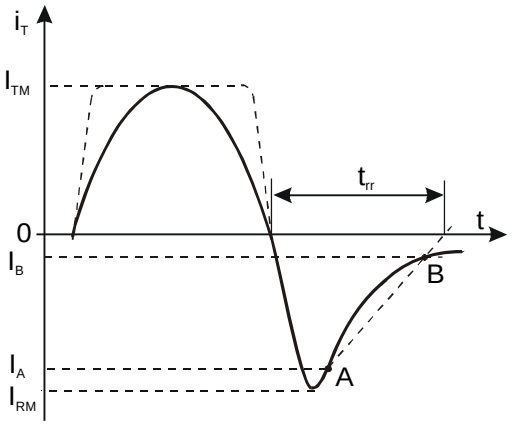
NOTE 1 The extrapolation is carried out with respect to specified points A and B, as shown in generalized form in figure 9b. Point A may be specified at I_{RM}.

NOTE 2 Specified values of t_{rr} refer to a specified waveform of the preceding on-state current pulse, which may be either a half sine wave (solid line) or a trapezoidal wave (dashed line).



IEC 2029/2000

Figure 9a – Determined by specified value



IEC 2030/2000

Figure 9b – Determined by extrapolation

Figure 9 – Reverse recovery time

3.9.12
off-state recovery time (of a reverse-conducting thyristor) (t_{dr})
The time interval between

– the instant when the current passes through zero while changing from the reverse-conducting state to the off state,

and

– the instant when either the off-state current is reduced from its peak value I_{DM} to a specified low value I_1 (as shown in figure 10a and which may be zero), or the extrapolated reverse current reaches zero (as shown in figure 10b).

NOTE 1 The extrapolation is carried out with respect to specified points A and B, as shown in generalized form in figure 10b. Point A may be specified at I_{DM}.

NOTE 2 Specified values of t_{dr} refer to a specified waveform of the preceding reverse-current pulse, which may be either a half sine wave (solid line) or a trapezoidal wave (dashed line).

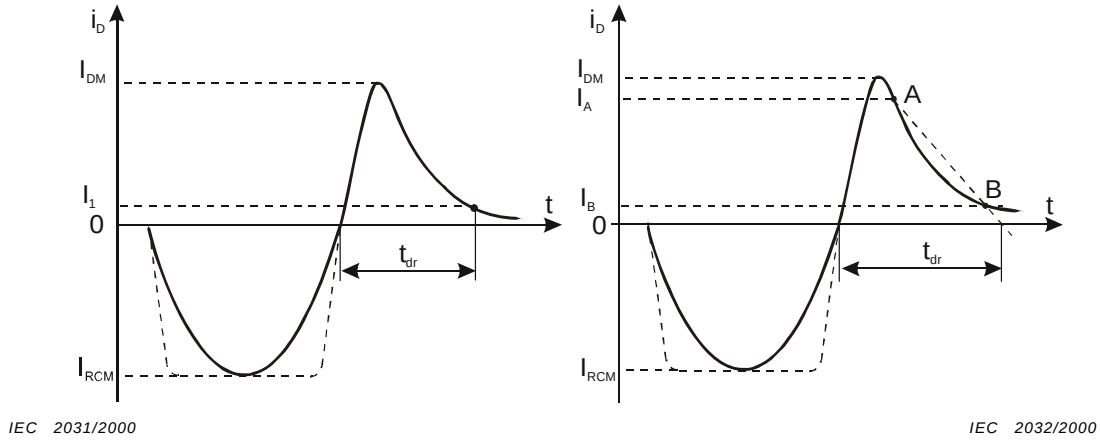


Figure 10a – Determined by specified value **Figure 10b – Determined by extrapolation**

Figure 10 – Off-state recovery time

3.9.13
circuit-commutated turn-off time (t_q)
time interval between

– the instant when the on-state current has decreased to zero after external switching of the main circuit, and

– the earliest instant when a steeply rising off-state voltage that the thyristor is capable of supporting without breaking over either passes through zero (curve a) in figure 11, or begins from a low positive value (curve b) in figure 11.

NOTE Curve a) refers to a simple reverse-blocking triode thyristor. Curve b) may appear, if the thyristor is bypassed by an external or internal inverse diode (reverse-conducting thyristor), due to the lead inductance of the diode.

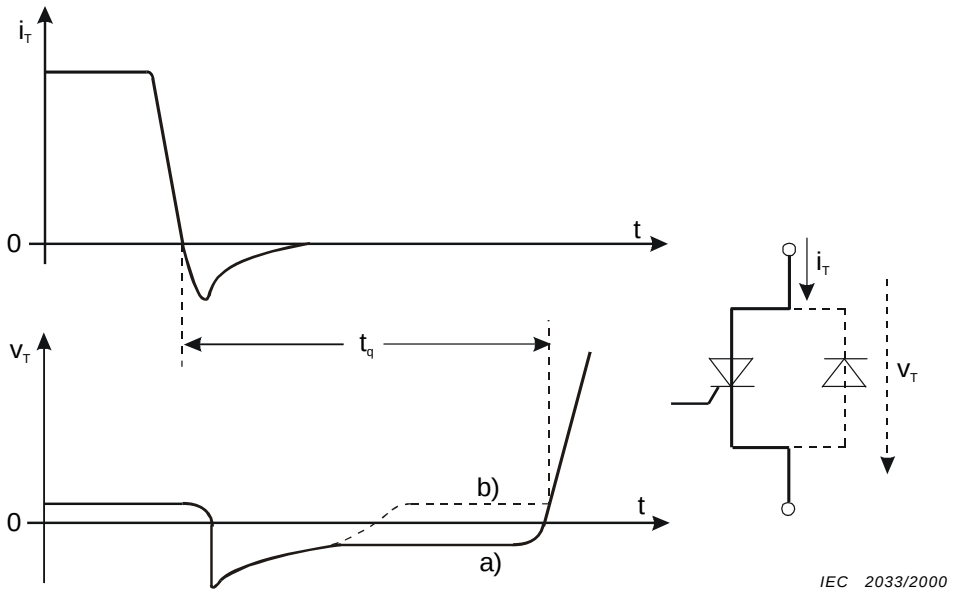


Figure 11 – Circuit-commutated turn-off time

3.9.14
hold-off interval (in a converter) (t_H)
time interval between

– the instant when the anode current of the thyristor of a converter has decreased to zero,

and

– the instant when the same thyristor is subjected to off-state voltage.

NOTE The hold-off interval is not a characteristic of the thyristor but a service condition of the converter. It will exceed the longest expected individual circuit-commuted turn-off time, which also depends on the service conditions of the converter.

G Times and rates of rise characterizing gate-controlled turn-on (see figure 12)

NOTE 1 The defined terms refer to the switching of a thyristor from the off state to the on state by means of a forward gate drive current pulse.

NOTE 2 The reference values of current and voltage referred to in the following subclauses are usually specified as follows:

gate current:

– specified low value: 10 % of I_{FGTM},
– specified level for the measurement of t_{gtw} and di_G/dt: 50 % of I_{FGTM},

anode voltage:

– upper specified value: 90 % of V_D,
– lower specified value: 10 % of V_D, (where V_D is the off-state voltage prior to turn on),

anode current:

– specified level for the measurement of di_G/dt: 50 % of I_{TM}.

3.9.15
gate-controlled turn-on delay time (t_{gd})
time interval between

– the instant when the rising gate drive current pulse reaches a specified low value, and

– the instant when the decreasing off-state voltage reaches an upper specified value near its initial value V_D.

NOTE If no ambiguity is likely to occur, the term may be abbreviated to “turn-on delay time”.

3.9.16
gate-controlled turn-on rise time (t_{gr})
time interval between

– the instant when the off-state voltage reaches the upper specified value referred to in 3.9.15, and

– the instant when the decreasing off-state voltage reaches a lower specified value near its final steady-state value

NOTE If no ambiguity is likely to occur, the term may be abbreviated to “turn-on rise time”.

3.9.17
gate-controlled turn-on time (t_{gt})
sum of gate-controlled turn-on delay time and rise time:

$$t_{gt} = t_{gd} + t_{gr}$$

NOTE If no ambiguity is likely to occur, the term may be abbreviated to “turn-on time”.

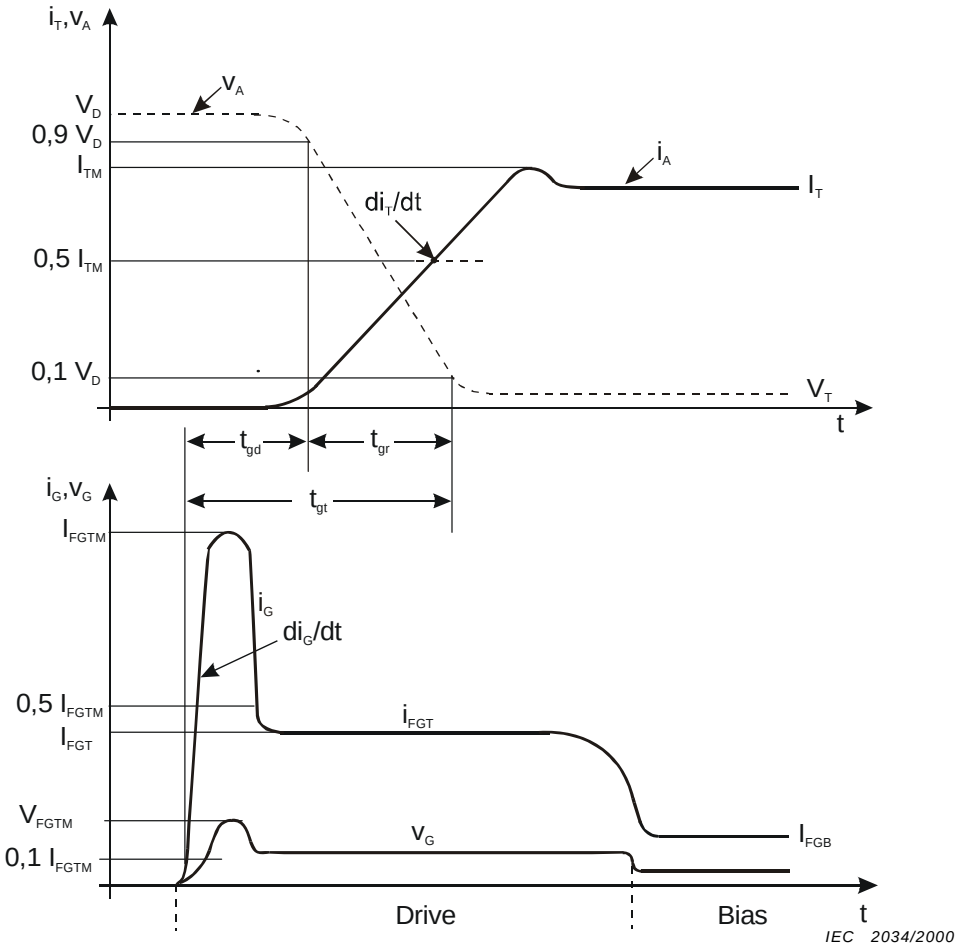


Figure 12 – Gate-controlled turn-on times

3.9.18
gate turn-on drive-pulse duration (t_{gtw})
duration of the forward gate drive current pulse measured between two specified levels of the forward gate current

3.9.19
critical gate turn-on drive-pulse duration ($t_{gtw(cr)}$)
lowest value to which the gate turn-on drive pulse duration can be reduced without the thyristor failing to turn on

H Times and rates of rise characterizing, gate-controlled turn-off (see figure 13)

NOTE 1 The defined terms refer to the switching of a GTO thyristor from the on state to the off state by means of a reverse gate drive current pulse that is supported by an additional reverse gate drive voltage pulse and that is followed by a smaller reverse gate bias current.

NOTE 2 The reference values of current and voltage referred to in 3.9.20 through 3.9.25 are usually specified as follows:

gate current:
– specified low value near zero: 10 % of I_{RGQM},
– specified level for the measurement of di_{RG}/dt: 50 % of I_{RGQM},

anode current:
– upper reference value: 90 % of I_T,

anode voltage:
– specified level for the measurement of dv_D/dt: 50 % of V_{DQM}.

3.9.20
gate-controlled turn-off delay time (t_{dq})
time interval between

– the instant when the rising reverse gate current reaches a low reference value near zero, and

– the instant when the anode current has decreased to an upper reference value near its initial value I_T.

NOTE If no ambiguity is likely to occur, the term may be abbreviated to “turn-off delay time”.

3.9.21
gate-controlled fall time (t_{fq})
time interval between

– the instant when the anode current has decreased to the upper reference value referred to in 3.9.20, and

– the instant when the anode current reaches, at the end of its steep decrease, the valley point current I_{ZV}

NOTE If no ambiguity is likely to occur, the term may be abbreviated to “turn-off fall time”.

3.9.22
gate-controlled turn-off time (t_{gq})
sum of gate-controlled turn-off delay time and fall time:

$$t_{gq} = t_{dq} + t_{fq}$$

NOTE If no ambiguity is likely to occur, the term may be abbreviated to “turn-off time”.

3.9.23
tail time (t_z)
time interval between

– the instant when the anode current has decreased to the valley point I_{ZV}, referred to in 3.9.21, and

– the instant when the extrapolated tail current reaches zero.

NOTE Unless otherwise specified, the extrapolation is carried out between the peak point of the tail current I_{ZM} and I_{ZL} = 25 % I_{ZM} (see figure 13).

3.9.24
gate turn-off drive-pulse duration (t_{pgq})
duration of the reverse gate-drive voltage pulse measured between two specified levels of reverse gate-drive voltage

3.9.25
critical gate turn-off drive-pulse duration ($t_{pgq(cr)}$)
lowest value to which the gate turn-off drive-pulse duration can be reduced without the thyristor failing to turn off

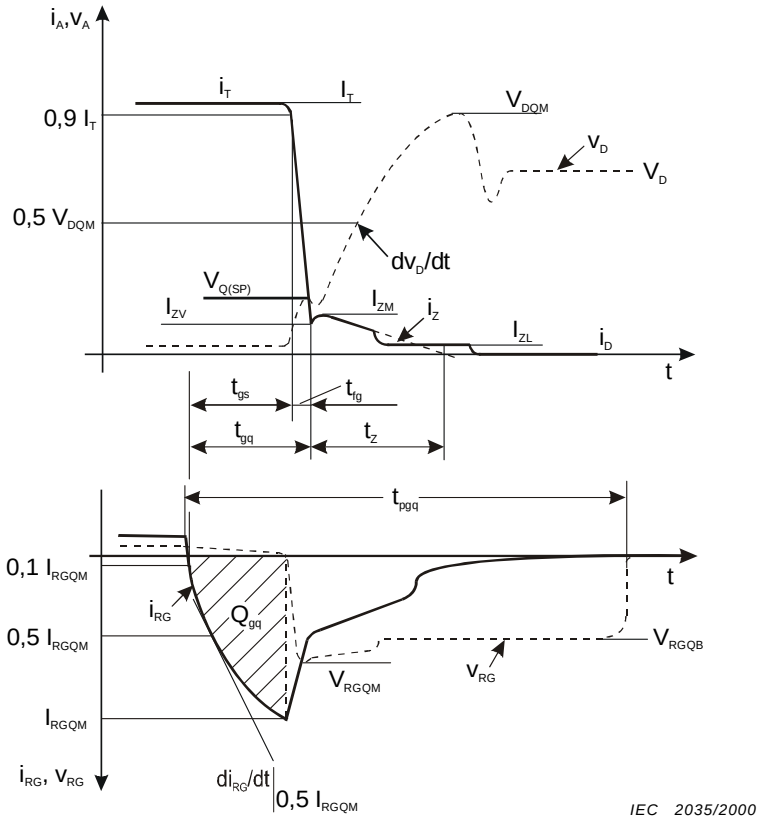


Figure 13 – Gate-controlled turn-off times

I Recovered charges

3.9.26
recovered charge(of a reverse-blocking triode thyristor) (Qr)
total charge recovered from the thyristor during a specified integration time after switching from a specified on-state current condition to a specified reverse condition:

$$Q_r = \int_{t_0}^{t_0 + t_i} i_R \, dt$$

where

t_0 is the instant when the current passes through zero;

t_i is the specified integration interval (see figure 14).

NOTE This charge includes components due to both carrier storage and depletion layer capacitance.

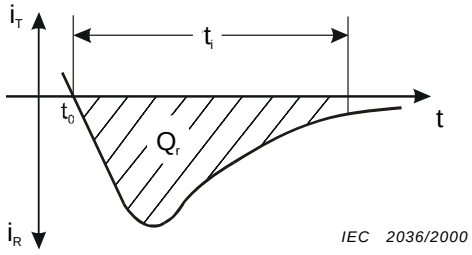


Figure 14 – Recovered charge Q_r

3.9.27
off-state recovered charge (of a reverse-conducting triode thyristor) (Q_{dr})
total charge recovered from the thyristor during a specified integration time after switching from a specified reverse current condition to a specified off-state condition

NOTE The formula given in 3.9.26 and figure 14 apply analogously.

3.9.28
gate turn-off charge (of a GTO thyristor) (Q_{gq})
total charge derived from the integration of the reverse gate current between the instant when the falling forward gate current crosses zero and the instant in which the reverse gate current reaches its peak value I_{RGQM} (see figure 13)

4 Letter symbols

4.1 General

The general rules of IEC 60747-1, chapter V, are applicable in part.

4.2 Additional general subscripts

In addition to the lists of recommended general subscripts given in IEC 60747-1, chapter V, the following special subscripts are recommended for the field of thyristors.

Subscript	Significance	Remarks
A, a	Anode	
B	Bias	As last subscript only
B	Basic	As last subscript only
(BO)	Breakover	
(com)	Commutating	As for fourth subscript only
D,d	Off-state	In $R_{th(j-c)D}$ only
D	Drive	
D	Diode	
G,g	Gate	
G	Gate-controlled	
H	Holding	
h	Hold-off	
K, k	Cathode	
L	Latching	
Q, q	Turn-off	
R, (REC)	Reverse recovery	In I_{RM} or $I_{R(REC)}$ and $I_{RM(REC)}$ only
RC	Reverse-conducting	
(SP)	Spike	
Sus	Sustaining	
T	On state	
T, t	Turn-on, trigger	
T	Thyristor	
V	Valley	
W	Working	
Z, z	Tail	

4.3 List of letter symbols

The symbols contained in the following lists are recommended for use in the field of thyristors; they have been compiled in accordance with the general rules.

4.3.1 Principal voltages, anode-cathode voltages

Name and designation	Letter symbol	Remarks
Off-state voltage	V_D	
Direct off-state voltage	$V_{D(D)}$	
Peak off-state voltage	V_{DM}	
Crest (peak) working off-state voltage	V_{DWM}	
Repetitive peak off-state voltage	V_{DRM}	
Non-repetitive peak off-state voltage	V_{DSM}	
Breakover voltage	$V_{(BO)}$	
On-state voltage	V_T	
Minimum on-state voltage	V_{TMIN}	
On-state threshold voltage	$V_{T(TO)}$	
Reverse voltage	V_R	
Direct reverse voltage	$V_{R(D)}$	
Crest (peak) working reverse voltage	V_{RWM}	
Repetitive peak reverse voltage	V_{RRM}	
Non-repetitive peak reverse voltage	V_{RSM}	
Reverse breakdown voltage	$V_{(BR)}$	
Reverse-conducting threshold voltage	$V_{RC(TO)}$	

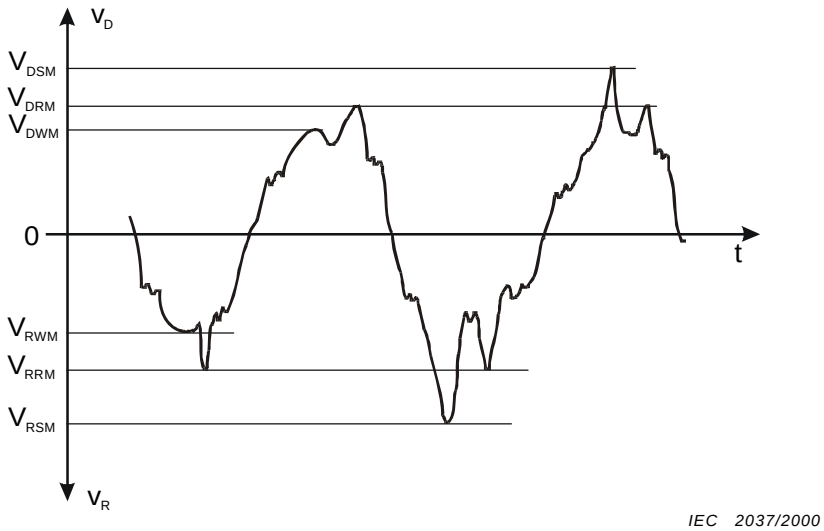


Figure 15 – Letter symbols for rated off-state reverse voltages

4.3.2 Principal currents, anode currents, cathode currents

Name and designation	Letter symbol	Remarks
Off-state current	I_D	
Breakover current	$I_{(BO)}$	
Holding current	I_H	
On-state current	I_T	
Overload on-state current	$I_{(OV)}$	
Repetitive peak on-state current	I_{TRM}	
Surge (non-repetitive) on-state current	I_{TSM}	
Reverse blocking current	I_R	
Repetitive peak reverse current	I_{RRM}	
Reverse recovery current	I_{RR}	
Peak reverse recovery current	I_{RM}	
Latching current	I_L	
Reverse-conducting current	I_{RC}	
Mean reverse-conducting current	$I_{RC(AV)}$	
Peak reverse-conducting current	I_{RCM}	
Overload reverse-conducting current	$I_{RC(OV)}$	
Surge reverse-conducting current	I_{RCSM}	
Direct on-state current	$I_{T(D)}$	
Direct off-state current	$I_{D(D)}$	

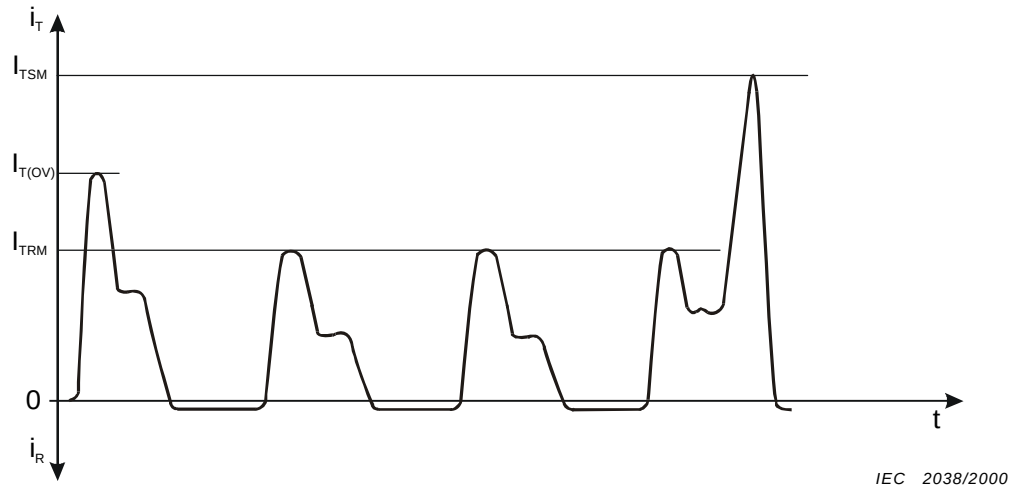


Figure 16 – Letter symbols for on-state current ratings

4.3.3 Gate voltages

Name and designation	Letter symbol	Remarks
Forward gate continuous (direct)voltage	V_{FG}	
Peak forward gate voltage	V_{FGM}	
Reverse gate continuous (direct) voltage	V_{RG}	
Peak reverse gate voltage	V_{RGM}	
Gate trigger continuous (direct) voltage	V_{GT}	
Minimum gate trigger voltage	V_{GTMIN}	
Gate non-trigger continuous (direct) voltage	V_{GD}	
Gate turn-off continuous (direct) voltage	V_{GQ}	

4.3.4 Gate currents

Name and designation	Letter symbol	Remarks
Forward gate continuous (direct) current	I_{FG}	
Peak forward gate current	I_{FGM}	
Reverse gate continuous (direct) current	I_{RG}	
Gate trigger continuous (direct) current	I_{GT}	
Gate non-trigger continuous (direct) current	I_{GD}	
Gate turn-off continuous (direct) current	I_{GQ}	

4.3.5 Time quantities

Name and designation	Letter symbol	Remarks
Gate controlled turn-on time	t_{gt}	
Gate controlled turn-off time	t_{gq}	
Circuit commutated recovery time (circuit commutated turn-off time)	t_q	
Gate-controlled delay time	t_{gd},(t_d)	t_d and t_r shall be used only when misinterpretation will not result
Gate-controlled rise time	t_{gr}, (t_r)	t_d and t_r shall be used only when misinterpretation will not result
Off-state recovery time	t_{dr}	For reverse conducting triode thyristors
Hold-off interval	t_H	

4.3.6 Sundry quantities

Name and designation	Letter symbol	Remarks
On-state slope resistance	r_T	
Critical rate of rise of commutating voltage	dv/dt(c), (dv/dt(com))	For reverse conducting triode thyristors, dv/dt(c) is the preferred symbol
Off-state recovered charge	Q_{dr}	For reverse conducting triode thyristors
Total energy of on-state current pulse	E_P W_p	
Reverse-conducting slope resistance	r_{RC}	

4.3.7 Power loss

Name and designation	Letter symbol	Remarks
On-state power loss	P_T	
Reverse power loss	P_R	For reverse blocking and conducting triode thyristors
Off-state power loss	P_D	
Turn-on loss – average turn-on loss – total instantaneous turn-on loss – peak turn-on loss	 $P_{TT(AV)}$ P_{TT} P_{TTM}	
Turn-off loss – average turn-off loss – total instantaneous turn-off loss – peak turn-off loss	 $P_{RQ(AV)}$ or $P_{DQ(AV)}$ P_{RQ} or P_{DQ} P_{RQM} or P_{DQM}	
Reverse-conducting power loss	P_{RC}	

5 Essential ratings and characteristics for reverse-blocking and reverse-conducting triode thyristors

This clause gives standards for (symmetrical and asymmetrical) reverse-blocking triode thyristors and for reverse-conducting triode thyristors. The ratings and characteristics are specified for reverse-blocking thyristors but most of them may be applied also to reverse-conducting thyristors.

The term “reverse-blocking triode thyristor” has been abbreviated in the text to “thyristor”.

5.1 Thermal conditions

Thyristors shall be specified as ambient-rated devices or as case-rated devices.

At higher frequencies, the current ratings of fast-switching thyristors depend on the on-state, turn-on. turn-off and gate power dissipation in a rather complicated way. Therefore, ratings dependent on frequency are necessary.

Besides the current ratings given for a specified case temperature, the average power dissipation must be known in order to calculate the cooling conditions necessary. For this calculation, the average power dissipation or the total energy dissipation for one pulse shall be given. If the energy dissipation per pulse is given, the average power dissipation is obtained by multiplying it by the repetition frequency.

5.1.1 Recommended temperatures

Many of the ratings and characteristics are required to be quoted at a temperature of 25 °C and at one other specified temperature. Unless otherwise stated, the one other specified temperature shall be chosen by the manufacturer from the list in IEC 60747-1; in addition, temperatures of –40 °C and +35 °C may be used.

5.1.2 Rating conditions

The ratings shall be stated under one or more of the following thermal conditions.

A Ambient-rated thyristors

– Natural convection

At 25 °C and at one higher temperature (see 5.1.1). The cooling fluid and pressure (in the case of a gas) shall be specified.

Air pressure shall be at least 90 kPa (900 mbar), corresponding to a maximum level of 1 000 m above sea level.

– Forced circulation

At a temperature taken from the list of recommended temperatures (see 5.1.1). The type, pressure and flow of the cooling fluid shall be specified.

B Case-rated thyristors

At a case temperature taken from the list of recommended temperatures (see 5.1.1).

NOTE For small thyristors the temperature on one of the terminals may be specified.

5.2 Voltage and current ratings (limiting values)

The following ratings must be valid for the whole range of operating conditions as stated for the particular device.

A Anode-cathode voltages

5.2.1 Non-repetitive peak reverse voltage (V_{RSM})

Maximum rated value. If this value has to be derated at higher operating frequencies, the derating factor or curve shall be given.

5.2.2 Repetitive peak reverse voltage (V_{RRM})

Maximum rated value. If this value has to be derated at higher operating frequencies, the derating factor or curve shall be given.

5.2.3 Crest (peak) working reverse voltage (V_{RWM}) (where appropriate)

Maximum rated value of a repetitive reverse voltage having a half wave sinusoidal wave-form at mains frequency, usually 50 Hz or 60 Hz (duration: 10 ms or 8,3 ms).

5.2.4 Continuous (direct) reverse voltage (V_R) (where appropriate)

Maximum rated value.

5.2.5 Non-repetitive peak off-state voltage (V_{DSM})

Maximum rated value. If this value has to be derated at higher operating frequencies, the derating factor or curve shall be given.

5.2.6 Repetitive peak off-state voltage (V_{DRM})

Maximum rated value. If this value has to be derated at higher operating frequencies, the derating factor or curve shall be given.

5.2.7 Crest (peak) working off-state voltage (V_{DWM}) (where appropriate)

Maximum rated value of a repetitive off-state voltage having a half wave sinusoidal waveform at mains frequency, usually 50 Hz or 60 Hz (duration: 10 ms or 8,3 ms).

5.2.8 Continuous (direct) off-state voltage (V_D) (where appropriate)

Maximum rated value under specified conditions of control signal and gate circuit impedance.

B Gate voltages

Gate voltages are applied between gate and cathode terminals of a P-gate thyristor (gate positive for a forward gate voltage), and between anode and gate terminals of an N-gate thyristor (anode positive for a forward gate voltage).

5.2.9 Peak forward gate voltage (anode positive with respect to cathode) (V_{FGM})

Maximum rated value.

5.2.10 Peak forward gate voltage (anode negative with respect to cathode) (V_{FGM})

Maximum rated value.

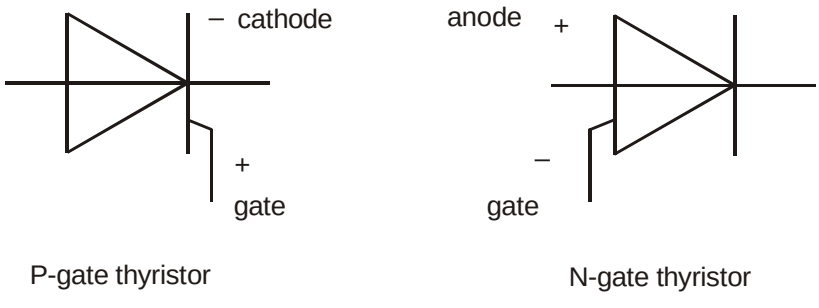


Figure 17 – Application of gate voltages for thyristors

5.2.11 Peak reverse gate voltage (V_{RGM}) (where appropriate)

Maximum rated value.

C On-state current

5.2.12 Mean on-state current

The maximum rated values shall be specified in a diagram showing the mean on-state current for continuous operation with half sine waves of 180° conduction angle and with rectangular pulses of various conduction angles, at least 180° and 120°, at 50 Hz or 60 Hz, versus ambient or case temperature.

As a reference value for certain characteristics (see 5.4), the maximum rated value for half sine waves of 180° conduction angle at 45 °C ambient or 85 °C case temperature should be given as an example.

NOTE The maximum rated value of the mean on-state current is given on the assumption that no overload occurs.

5.2.13 Repetitive peak on-state current (where appropriate)

Maximum rated value for continuous operation. This rating shall be expressed with relation to the on-state current conduction angle, cooling conditions and operating frequency.

5.2.14 RMS on-state current (where appropriate)

Maximum rated value for continuous operation.

5.2.15 Overload on-state current (where appropriate)

This rating shall be given by stating the maximum rated virtual junction temperature and the maximum transient thermal impedance. In addition, overload current ratings may be given by means of diagrams.

5.2.16 Surge on-state current

This rating shall be given at initial conditions corresponding to maximum rated virtual junction temperature. In addition, figures corresponding to lower initial virtual junction temperatures may be given.

Surge current ratings shall be given for the following time periods:

a) for times smaller than one half cycle (at 50 Hz or 60 Hz), but greater than approximately 1 ms, in terms of maximum rated value of

$$\int i^2 dt$$

These ratings may be given by means of a curve or by specified values. No immediate subsequent application of reverse voltage or off-state voltage is assumed.

NOTE For fast turn-on thyristors or fast plasma-spreading thyristors such as those with distributed gate or inter-digitated gate structures, values for times below 1 ms may be needed.

b) for times equal to, or greater than, one half cycle and smaller than 15 cycles (at 50 Hz or 60 Hz), in the form of a curve showing the maximum rated surge current versus time. Temporary loss of gate control shall be assumed to occur.

   These ratings should preferably be given for a reverse voltage of 80 % of the maximum repetitive peak reverse voltage. Additional ratings may be given for reverse voltages of 50 % or 100 % of the maximum repetitive peak reverse voltage.

c) for a time equal to one cycle, with no reverse voltage applied.

5.2.17 Continuous (direct) on-state current (where appropriate)

Maximum rated value.

5.2.18 Peak value of sinusoidal on-state current at higher frequencies (where appropriate)

Curves showing the maximum rated peak on-state current values as functions of the half sine wave current pulse duration, with the repetition frequency as a parameter, under the following conditions:

a) specified case temperature;

b) specified off-state voltage before turn-on;

c) specified reverse voltage;

d) specified gate conditions during turn-on and turn-off;

e) specified RC damping network (snubber).

Figure 18a is given as an example. Figure 18b is given for explanatory purposes only.

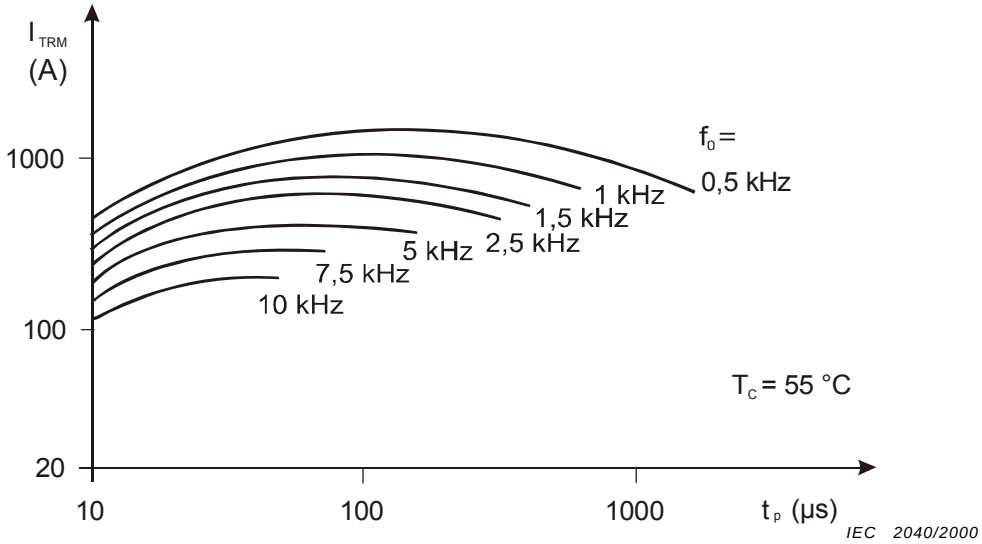
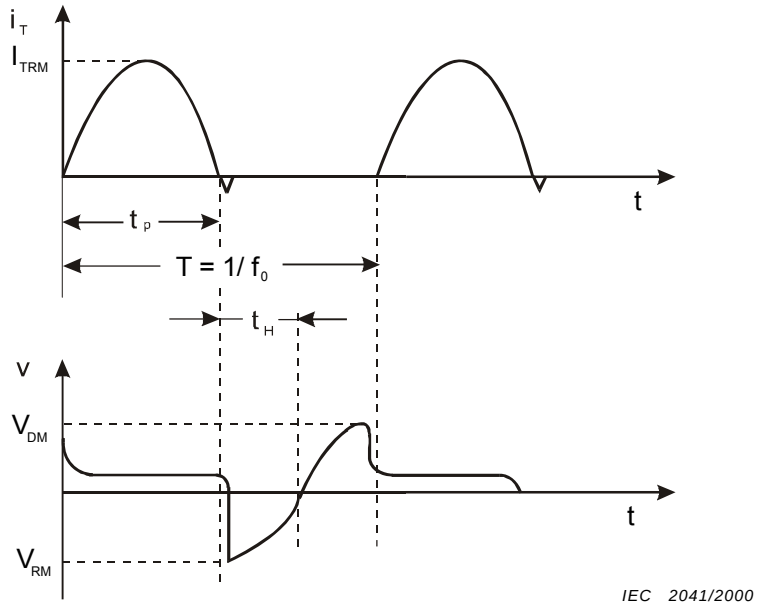


Figure 18a – Maximum rated peak sinusoidal on-state current I_{TRM} (see figure 18b) as a function of pulse duration t_p with parameter: repetition frequency $f_0 = 1/T$



NOTE The pulse waveform includes the current pulse due to the RC damping network.

Figure 18b – Typical current and voltage waveforms for sinusoidal on- state current pulses; t_H is the hold-off interval (see 3.9.14)

Figure 18 – Maximum rated peak sinusoidal on-state current

5.2.19 Peak value of a trapezoidal on-state current at higher frequencies (where appropriate)

Curves showing the maximum rated on-state current values related to the rate of rise of on-state current, the repetition frequency and either the duty cycle or pulse duration under the following conditions:

a) specified case temperature;

b) specified off-state voltage before turn-on;

c) specified reverse voltage;

NOTE As there is a significant dependence on the applied reverse voltage, it is recommended that two or more families of curves be given.

d) specified gate conditions during turn-on and turn-off;

e) specified RC damping network (snubber);

f) specified duty cycle or pulse duration.

Figures 19a and 19b are given as examples. Figure 19c is given for explanatory purposes only.

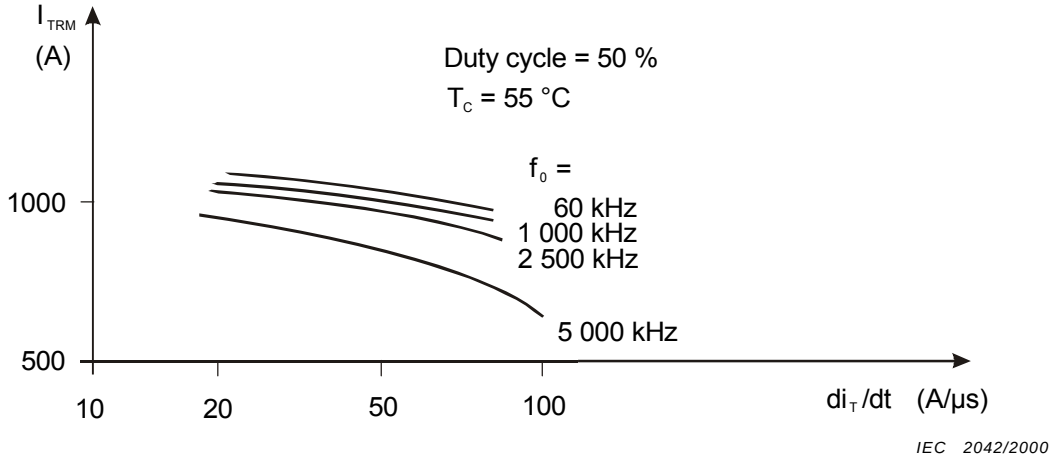
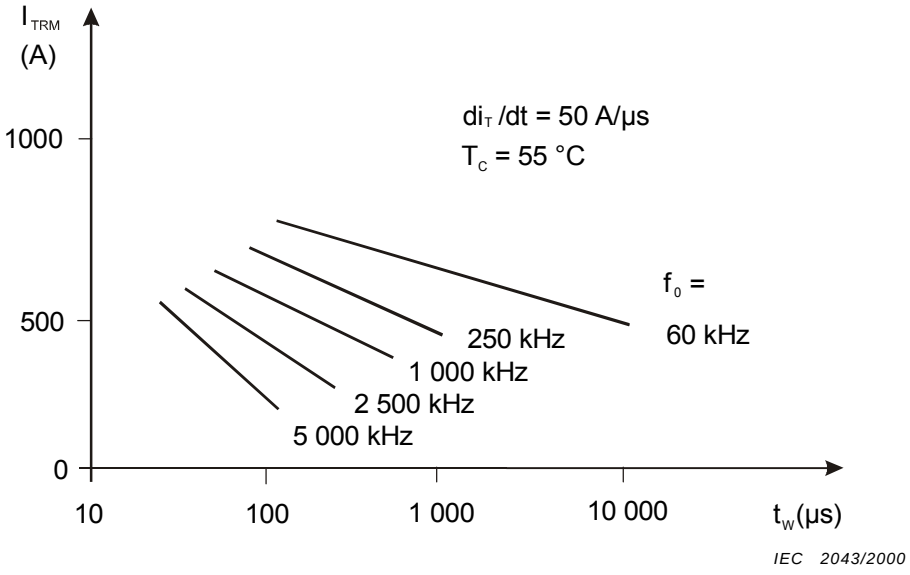


Figure 19a – Maximum rated peak trapezoidal on-state current I_{TRM} for a specified t_w (see figure 19c) as a function of the rate of rise of on-state current with parameter repetition frequency $f_0 = 1/T$



NOTE Different sets of curves are required for different values of di_T/dt.

Figure 19b – Maximum rated peak trapezoidal on-state current I_{TRM} having a specified di_T/dt (see figure 19c) as a function of t_w with parameter: repetition frequency $f_0 = 1/T$

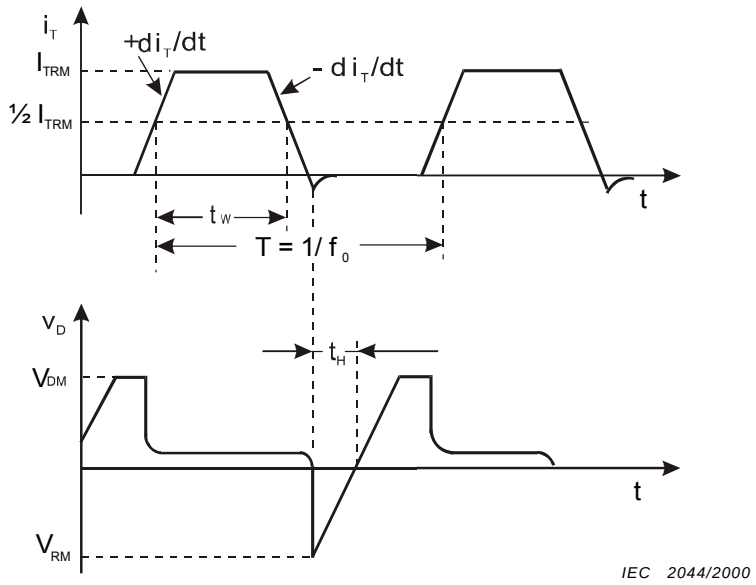


Figure 19c – Typical current and voltage waveforms for trapezoidal on-state current pulses; t_H is the hold-off interval (see 3.9.14)

Figure 19 – Peak value of a trapezoidal on-state current

5.2.20 Critical rate of rise of on-state current

Maximum rated value under the following specified conditions:

a) off-state voltage (prior to turn-on), preferably equal to two-thirds of the maximum rated repetitive peak off-state voltage;

b) peak value of on-state current;

c) repetition rate, preferably 50 Hz or 60 Hz;

d) ambient or case temperature, equal to the highest temperature at which the peak value of on-state current is permitted;

e) gate-trigger conditions;

f) test duration (the duration shall be longer than the thermal time constant of the device, for example, 5 s).

NOTE 1 di/dt ratings are not applicable to low-current thyristors.

NOTE 2 The rated value of di/dt should be given for the case of no RC network connected in parallel with the thyristor. If an additional di/dt rating is given for the case where an RC network is present, the permissible amplitude and duration of the surges from this network or the parameters of this network must be stated.

5.2.21 Peak case non-rupture current

The limiting value “peak case non-rupture current” shall be specified, where appropriate, as the maximum value of a triangular current rising at a specified rate, preferably 25 A/µs, and having a specified pulse duration for a starting case temperature to be specified, preferably 25 °C.

NOTE 1 The “peak case non-rupture current” is needed for high-current thyristors (mean current ratings of about 1 000 A and higher) that are used in large converter installations (as a rule, several devices are connected in parallel), where a device failing to block reverse voltage causes a high, steeply rising short-circuit current that can fracture the case and cause damage to the equipment before a fuse has time to operate.

NOTE 2 Therefore, the determination or verification of this limiting value of current needs a high-power testing facility, and the costs of the testing itself and of the samples which are destroyed in the test are considerable and are justified only in cases where the above danger really exists.

NOTE 3 The value of the peak case non-rupture current depends considerably on the location of the initial breakdown, on the silicon chip and is usually lowest if the breakdown occurs near the edge.

D Gate current

5.2.22 Peak forward-gate current

Maximum rated value, with anode-cathode voltage polarity specified.

NOTE Any qualifications (for example, of time, energy, etc.) applicable to this rating must be stated.

5.3 Other ratings (limiting values)

5.3.1 Frequency ratings

Where applicable, the maximum and/or minimum frequencies for which the voltage and current ratings apply.

A Power dissipation ratings

5.3.2 Peak gate power dissipation

Maximum rated value for specified pulse duration.

B Temperature ratings

5.3.3 Ambient-rated and case-rated thyristors

Minimum and maximum rated cooling fluid or case temperatures.

5.3.4 Storage temperatures

Minimum and maximum rated values.

5.3.5 Virtual junction temperature (where appropriate)

Maximum rated value.

5.4 Electrical characteristics

(At ambient or case temperature of 25 °C, unless otherwise stated.)

5.4.1 On-state characteristics (where appropriate)

Curves showing instantaneous values of on-state voltage versus on-state current up to the maximum rated value of the peak repetitive on-state current, at an ambient or case temperature of 25 °C and at one other higher temperature, preferably equal to the maximum rated virtual junction temperature.

5.4.2 On-state voltage

Maximum value at a current of s times the rated mean on-state current at the maximum rated virtual junction temperature or at a case or ambient temperature of 25 °C.

NOTE 1 s may be taken as equal to 3.

NOTE 2 The reference value for calculating the on-state power dissipation under operating conditions is the on-state voltage at maximum virtual junction temperature. If, however, a well-established correlation exists between this value and the value at 25 °C, the latter may be given for convenience of testing.

5.4.3 Holding current

Maximum value and, where appropriate, minimum value under the following specified conditions:

a) source voltage in the principal circuit, preferably equal to 12 V;

b) gate-bias conditions;

c) peak initial on-state current.

NOTE The maximum value of the holding current is the smallest current that will maintain all thyristors of a given type in the on state.

The minimum value of the holding current is the highest current below which all thyristors of a given type will return to the off state.

5.4.4 Latching current

Maximum value under the following specified conditions:

a) source voltage in the principal circuit, preferably equal to 12 V;

b) triggering pulse: rise time, fall time, duration, amplitude, and resistance of the trigger pulse generator.

NOTE The maximum value of the latching current is the smallest current that will maintain all thyristors of a given type in the on state immediately after the triggering condition has been removed.

5.4.5 Repetitive peak off-state current

Maximum value at the rated repetitive peak off-state voltage at 25 °C and, where appropriate, at the maximum rated virtual junction temperature.

5.4.6 Repetitive peak reverse current

Maximum value at the maximum rated repetitive peak reverse voltage at 25 °C; in addition, where appropriate, maximum value at the maximum rated virtual junction temperature.

5.4.7 Gate-trigger current and gate-trigger voltage

Values of gate current and gate voltage required to turn on all thyristors of a given type.

The following conditions shall be specified:

a) off-state voltage, preferably equal to 12 V;

b) gate-circuit conditions;

c) ambient or case temperature.

5.4.8 Gate non-trigger current and gate non-trigger voltage

Values of the gate current and gate voltage which will not turn on any thyristor of a given type.

The following conditions shall be specified:

a) off-state voltage, preferably equal to two-thirds of the maximum rated repetitive peak off-state voltage (V_{DRM});

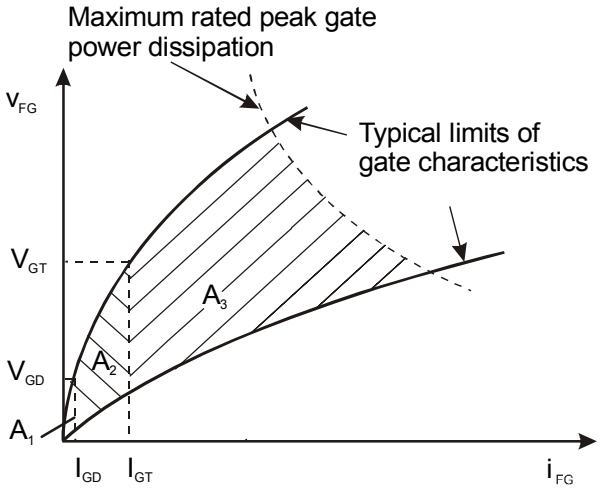
b) ambient or case temperature, preferably equal to the maximum rated virtual junction temperature;

c) gate circuit conditions.

Presentation of limiting values and characteristics for the gate

Limiting values and characteristics for the gate are preferably given with reference to a diagram as shown in figure 20. The area indicating certain triggering has a lower limit given by the gate trigger current.

NOTE The values of gate non-trigger voltage and current should be given at maximum rated virtual junction temperature. The values of gate-trigger voltage and current should be given at 25 °C and at minimum operating temperature.



I_{GD}	gate non-trigger current	A_1	area of non-triggering
I_{GT}	gate-trigger current	A_2	area of uncertain triggering
V_{GD}	gate non-trigger voltage	A_3	area of certain triggering
V_{GT}	gate-trigger voltage		

Figure 20 – Forward gate voltage versus forward gate current

5.4.9 Gate-controlled turn-on delay time

Typical and, where appropriate, maximum and/or minimum value(s), under the following specified conditions:

a) gate-current amplitude and gate-circuit impedance;

b) rise time of the gate pulse, preferably 0,5 µs;

c) minimum duration of the gate pulse, preferably two times the specified delay time;

d) off-state voltage (prior to turn-on), preferably equal to 0,5 times the maximum rated repetitive peak off-state voltage.

5.4.10 Circuit commutated turn-off-time

Maximum value under the following specified conditions:

a) waveshape of the preceding on-state current;

NOTE 1 The waveshape shall preferably be rectangular and the duration must be sufficient to achieve charge carrier equilibrium. The amplitude shall be preferably three times the rated mean on-state current.

b) ambient or case temperature equal to the highest temperature at which the peak value of the on-state current is permitted;

c) waveshape of the reverse-blocking voltage;

d) reverse voltage at the time of initiation of off-state voltage (time instant t_1 in figure 21);

e) peak value and rate of rise of off-state voltage;

NOTE 2 The peak value of the off-state voltage shall be at least two-thirds of the rated repetitive peak off-state voltage.

f) gate bias while the thyristor is in the off state:
   – gate-source voltage,
   – gate-source impedance;

g) rate of fall of on-state current (–di/dt).

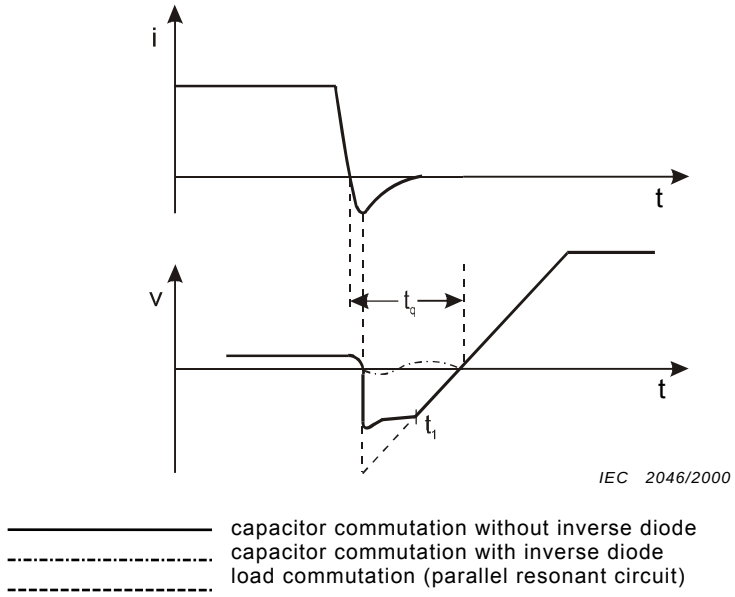


Figure 21 – Examples of current and voltage waveshapes during turn-off of a thyristor under various circuit conditions

5.4.11 Critical rate of rise of off-state voltage

Maximum value of the rate of rise of an applied voltage rising in an approximately linear manner.

The following conditions shall be specified:

a) ambient or case temperature, preferably equal to the maximum rated virtual junction temperature;

b) peak off-state voltage, preferably equal to two-thirds the maximum rated repetitive peak off-state voltage (V_{DRM});

c) specified waveform (linear or exponential);

d) gate-bias conditions;

e) switching repetition frequency.

5.4.12 Total power loss

For case-rated thyristors only, curves showing the maximum total power loss at maximum virtual junction temperature as a function of mean on-state current and conduction angle, at the maximum value of the repetitive peak reverse voltage and at the maximum value of the repetitive peak off-state voltage. A curve shall be given for each operating condition specified in 5.2.12.

5.4.12.1 Total energy loss during one half sine wave on-state current pulse (where appropriate)

Curves showing the maximum total loss of energy comprising turn-on plus on-state plus reverse recovery energy related to the peak on-state current and pulse duration under the following conditions:

NOTE 1 Curves for maximum total energy loss are given under conditions that cause the maximum operating junction temperature to be reached.

a) specified off-state voltage before turn-on;

b) specified reverse voltage;

NOTE 2 As there is a significant dependence on the reverse recovery loss, it is recommended that two or more families of curves be given based on different reverse voltages, in order to make it possible to calculate the reverse recovery loss.

c) specified gate conditions during turn-on and turn-off;

d) specified RC damping network (snubber).

Figure 22a is given as an example.

Figure 22b is given for explanatory purposes only.

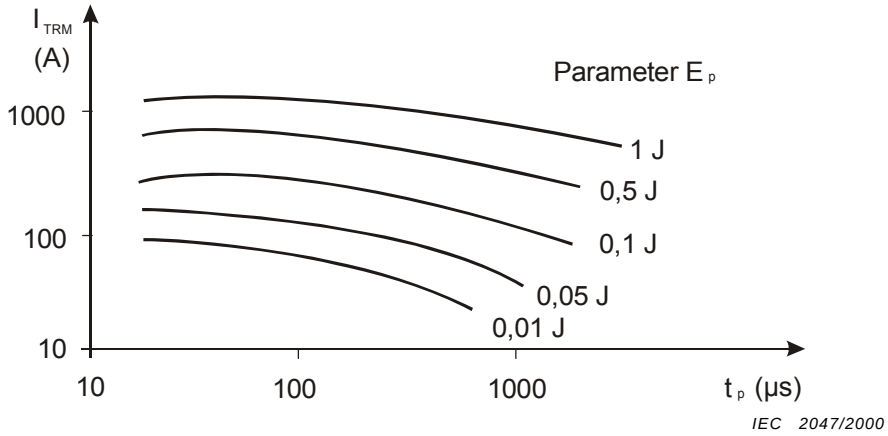


Figure 22a – Total energy loss E_p during a single half sine wave on-state current pulse of duration t_p and amplitude I_{TRM}

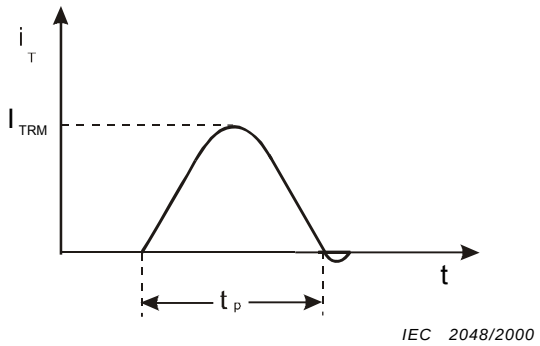


Figure 22b – Single sinusoidal on-state current pulse

Figure 22 – Total energy loss during one half sine wave on-state current pulse

5.4.12.2 Total energy loss during one trapezoidal on-state current pulse (E_p) (where appropriate)

Curves showing the maximum total dissipated energy values related to the maximum on-state current and the pulse duration under the following conditions:

a) specified off-state voltage before turn-on;

b) specified reverse voltage;

NOTE As there is a significant dependence on the reverse recovery loss, it is recommended that two or more families of curves be given based on different reverse voltages, in order to make it possible to calculate the reverse recovery loss.

c) specified gate conditions during turn-on and turn-off;

d) specified RC damping network (snubber);

e) specified rates of rise and decay of on-state current.

Figure 23a is given as an example.

Figure 23b is given for explanatory purposes only.

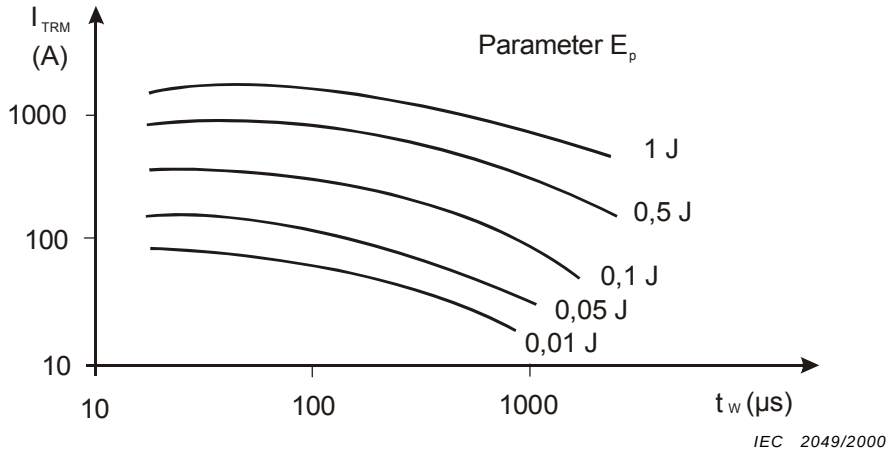


Figure 23a – Total energy loss E_p during a single trapezoidal on-state current pulse of duration t_W and amplitude I_{TRM}

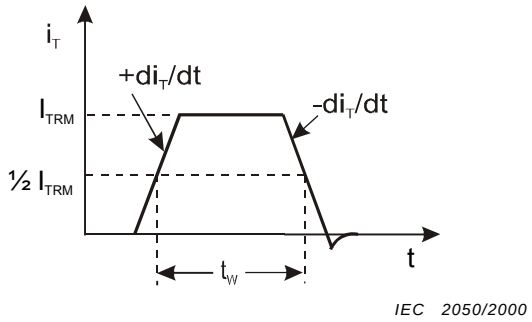


Figure 23b – Single trapezoidal on-state current pulse

Figure 23 – Total energy loss during one trapezoidal on-state current pulse

5.4.13 Recovered charge (Q_r) (where appropriate)

Maximum value, or maximum and minimum values, under the following specified conditions:

a) on-state current, preferably equal to the peak value of the maximum rated mean on-state current;

b) decay rate of on-state current –di/dt;

c) reverse voltage, preferably equal to 50 % of the maximum rated repetitive peak reverse voltage (V_{RRM}) as specified under 5.2.2;

d) ambient or case temperature equal to the highest temperature at which the peak value of the on-state current is permitted.

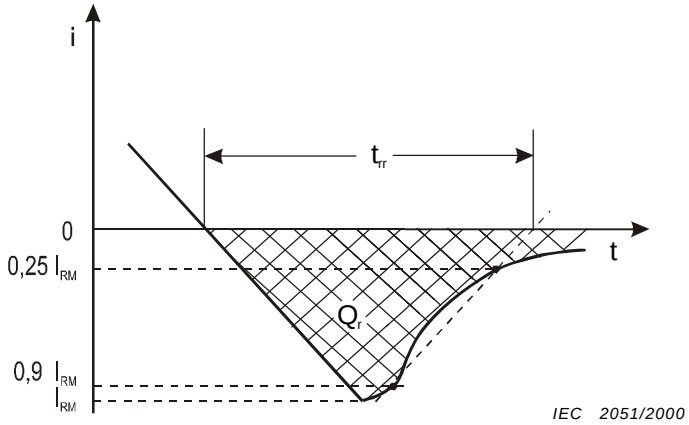


Figure 24 – Recovered charge Q_r, peak reverse recovery current I_{RM}, reverse recovery time t_{rr} (idealized characteristics)

5.4.14 Peak reverse recovery current (I_{RM})(where appropriate) – see figure 24 above

Maximum value under the same specified conditions a) to d) of 5.4.13.

5.4.15 Reverse recovery time (t_{rr}) (where appropriate) – see figure 24 above

Maximum value under the same specified conditions a) to d) of 5.4.13.

5.5 Thermal characteristics

5.5.1 Thermal resistance junction to ambient ($R_{th(j-a)}$)

Maximum value, for ambient rated thyristors only.

5.5.2 Thermal resistance junction to case ($R_{th(j-c)}$)

Maximum value, for case rated thyristors only.

5.5.3 Thermal resistance case to heatsink ($R_{th(c-h)}$)

Maximum value, for case rated thyristors only.

5.5.4 Thermal resistance junction to heatsink ($R_{th(j-h)}$)

Maximum value, for heatsink rated thyristors only.

5.5.5 Transient thermal impedance junction to ambient ($Z_{th(j-a)}$)

For ambient rated thyristors only, a curve of $Z_{th(j-a)}$ as a function of the time elapsed following a step change in power loss.

5.5.6 Transient thermal impedance junction to case ($Z_{th(j-c)}$)

For case rated thyristors only, a curve of $Z_{th(j-c)}$ as a function of the time elapsed following a step change in power loss.

5.5.7 Transient thermal impedance junction to heatsink ($Z_{th(j-h)}$)

For heatsink rated thyristors only, a curve of $Z_{th(j-h)}$ as a function of the time elapsed following a step change in power loss.

5.6 Mechanical characteristics and other data

See IEC 60747-1.

5.7 Application data

A statement of the special requirements that are applicable to series or parallel connection of thyristors or thyristor stacks.

The manufacturer should be consulted for detailed information.

6 Essential ratings and characteristics for bidirectional triode thyristors (triacs)

6.1 Thermal conditions

Triacs shall be specified as ambient rated devices or as case-rated devices or as heatsink rated devices.

6.1.1 Recommended temperatures

Many of the ratings and characteristics are required to be quoted at a temperature of 25 °C and at one other specified temperature.

Unless otherwise stated, the one other specified temperature shall be chosen by the manufacturer from the list in IEC 60747-1; in addition, temperatures of –40 °C and +35 °C may be used.

6.1.2 Rating conditions

The ratings shall be stated under one or more of the following thermal conditions.

A Ambient rated triacs

– Natural convection

  At 25 °C and at one higher temperature (see 6.1.1). The cooling fluid and pressure (in the case of a gas) shall be specified.

– Air pressure shall be at least 90 kPa (900 mbar), corresponding to a maximum level of 1 000 m above sea-level.

– Forced circulation

  At a temperature taken from the list of recommended temperatures (see 6.1.1). The type, pressure and flow of the cooling fluid shall be specified.

B Case rated or heatsink rated triacs

At a case temperature or heatsink temperature taken from the list of recommended temperatures (see 6.1.1).

NOTE For small triacs, the temperature on one of the terminals may be specified.

6.2 Voltage and current ratings (limiting values)

The following ratings shall be valid for the whole range of operating conditions as stated for the particular device.

The ratings and characteristics recommended here are based upon symmetrical operation of the device in either direction of the principal voltage. Therefore, equal limiting values should be given for either direction of operation. If a characteristic is sensitive to the gate-triggering mode, the mode(s) applicable shall be specified.

A Principal voltages

6.2.1 Non-repetitive peak off-state voltage (V_{DSM})

Maximum rated value.

If this value has to be derated at higher operating frequencies, the derating factor or curve shall be given.

6.2.2 Repetitive peak off-state voltage (V_{DRM})

Maximum rated value.

If this value has to be derated at higher operating frequencies, the derating factor or curve shall be given.

6.2.3 Crest (peak) working off-state voltage (V_{DWM})

Maximum rated value of a repetitive off-state voltage having a half wave sinusoidal wave-form at mains frequency, usually 50 Hz or 60 Hz (duration: 10 ms or 8,3 ms).

B Gate voltages

Gate voltages are applied between gate and main terminal 1 of the triac, with terminal 1 being the reference point for gate voltage polarity.

6.2.4 Peak positive gate voltage

Maximum rated value.

6.2.5 Peak negative gate voltage

Maximum rated value.

C Principal current

6.2.6 RMS on-state current

A curve showing maximum rated values versus ambient or case temperature or heatsink temperature for full sine waves and under phase control conditions. As a reference value for certain characteristics, the limiting value for full sine waves at 45 °C ambient or 85 °C case temperature or other specified temperature shall be given as an example.

NOTE The rated r.m.s. on-state current is given on the assumption that no overload occurs.

6.2.7 Repetitive peak on-state current (where appropriate)

Maximum rated value.

This rating shall be expressed in relation to the conduction angle.

6.2.8 Overload on-state current

Where this rating is appropriate, it shall be given by stating the maximum rated virtual junction temperature and the maximum transient thermal impedance. In addition, overload current ratings may be given by means of diagrams.

6.2.9 Surge on-state current

This rating shall be given at initial conditions corresponding to maximum rated virtual junction temperature. In addition, figures corresponding to lower initial virtual junction temperatures may be given.

Surge current ratings shall be given for the following time periods:

a) for times smaller than one half cycle (at 50 Hz or 60 Hz), but greater than approximately 1 ms, in terms of maximum rated value of

$$\int i^2 dt$$

These ratings may be given by means of a curve or by specified values. The rating applies for operation with either polarity of principal voltage. No immediate subsequent application of off-state voltage is assumed;

b) for times equal to or greater than one full cycle and smaller than 15 cycles (at 50 Hz or 60 Hz), in the form of a curve showing the maximum rated surge current versus time.

Temporary loss of gate control shall be assumed to occur.

These ratings are given for full cycles of 50 Hz or 60 Hz sine wave surge current.

6.2.10 Critical rate of rise of on-state current

Maximum rated value under the following specified conditions:

a) off-state voltage prior to turn-on, preferably equal to a half or two-thirds the maximum rated repetitive peak off-state voltage of 5.2.6;

b) peak value of on-state current, preferably equal to $\sqrt{2}$ times the rated r.m.s. on-state current of 5.2.12 specified at 85 °C for case or ambient temperature;

c) repetition rate, preferably 50 Hz or 60 Hz;

d) ambient or case temperature or junction temperature equal to the highest temperature at which the peak value of the on-state current is permitted;

e) gate-trigger conditions.

NOTE 1 The di/dt ratings are not applicable to low-current triacs.

NOTE 2 The rated value of di/dt should be given where there is no RC network connected in parallel with the triac. If an additional di/dt rating is given where an RC network is present, the permissible amplitude and duration of the surge from this network or the parameters of this network must be stated.

6.2.11 Gate currents

6.2.11.1 Peak positive gate current

Maximum rated value.

6.2.11.2 Peak negative gate current

Maximum rated value.

6.3 Other ratings (limiting values)

6.3.1 Frequency ratings

Where applicable, maximum and/or minimum frequencies for which the voltage and current ratings (subclause 6.2) apply.

A Power loss ratings – Gate power loss

6.3.2 Mean gate power

Maximum rated value.

6.3.3 Peak gate power

Maximum rated value.

If these ratings are temperature or duty factor dependent, derating information shall be given.

B Temperature ratings

6.3.4 Ambient-rated and case-rated triacs

Minimum and maximum rated ambient or case temperatures.

6.3.5 Storage temperatures

Minimum and maximum rated values.

6.3.6 Virtual junction temperature

Minimum and maximum rated value.

6.4 Electrical characteristics (at 25 °C ambient or case temperature, unless otherwise stated)

The characteristics recommended here are based upon symmetrical operation of the device, and therefore shall be based upon limiting values for either direction of operation. If a characteristic is sensitive to the gate triggering mode, the mode(s) applicable must be specified.

6.4.1 On-state characteristics (where appropriate)

Curves showing instantaneous value of on-state voltage versus on-state current up to the maximum rated value of the repetitive peak on-state current at an ambient or case temperature of 25 °C, and at one other higher temperature, preferably equal to the maximum rated virtual junction temperature.

This characteristic shall be measured using a pulse method, so that the junction temperature is approximately equal to the case temperature.

6.4.2 On-state voltage

Maximum value at a current of $\sqrt{2}$ times the maximum rated r.m.s. on-state current (5.2.12).

6.4.3 Holding current

Maximum and where, appropriate, minimum value under the following specified conditions:

a) off-state voltage, preferably equal to 12 V;

b) gate-bias conditions.

NOTE The maximum value of holding current is the smallest current that will maintain all triacs of a given type in the on state. The minimum value of holding current is the highest current below which all triacs of a given type will return to the off state.

6.4.4 Latching current

Maximum value under the following specified conditions:

a) off-state voltage, preferably equal to 12 V;

b) triggering pulse: rise time, fall time, duration, voltage, amplitude, and resistance of the pulse generator.

NOTE The maximum value of the latching current is the smallest current that will maintain all triacs of a given type in the on state immediately after the triggering condition has been removed.

6.4.5 Repetitive peak off-state current

Maximum value, at the maximum rated repetitive peak off-state voltage and at the maximum rated virtual junction temperature.

6.4.6 Critical rate of rise of off-state voltage

Maximum value of the rate of rise of an applied voltage rising in an approximately linear manner or in an exponential manner from zero to at least a half or two-thirds of the maximum rated repetitive peak off-state voltage, under specified switching repetition frequency, gate bias conditions and virtual junction temperature.

The following conditions shall be specified:

a) ambient or case temperature, preferably equal to the maximum rated virtual junction temperature;
b) peak off-state voltage, preferably equal to a half or two-thirds of the maximum rated repetitive peak off-state voltage (V_{DRM}) of 6.2.2;
c) gate bias conditions.

6.4.7 Critical rate of rise of commutating voltage

Maximum value under the following specified conditions:

a) peak on-state current preferably equal to $\sqrt{2}$ times the maximum rated r.m.s. value of on-state current of 6.2.6 at 25 °C for ambient-rated or at 85 °C for case-rated triacs;
b) duration (90 % of a half sine wave recommended) and rate of reversal of on-state current di/dt at zero crossing;
c) peak off-state voltage, preferably equal to a half or two-thirds of the maximum rated repetitive peak off-state voltage (V_{DRM}) of 5.2.6;
d) ambient or case temperature, preferably equal to the maximum rated virtual junction temperature;
e) gate bias conditions.

6.4.8 Gate trigger current and gate trigger voltage

Values of minimum gate current and minimum gate voltage required to turn on all triacs of a given type at specified low principal voltage.

The following conditions shall be specified:

a) off-state voltage, preferably 12 V;
b) gate-circuit conditions;
c) ambient or case or junction temperature.

Any other conditions affecting the values of these characteristics shall be specified.

6.4.9 Gate non-trigger current and gate non-trigger voltage

Values of maximum gate current and maximum gate voltage which will not turn on any triac of a given type at the rated repetitive peak off-state voltage.

The following conditions shall be specified:

a) off-state voltage, preferably equal to a half or two-thirds of the maximum rated repetitive peak off-state voltage (V_{DRM}) of 6.2.2;
b) ambient or case temperature, preferably equal to the maximum rated virtual junction temperature;
c) gate circuit conditions.

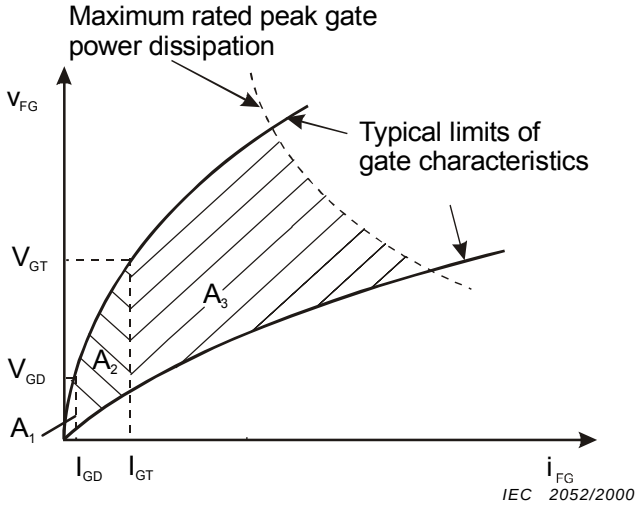
Any other conditions affecting the values of these characteristics shall be specified.

Presentation of limiting values and characteristics for the gate

Limiting values and characteristics for the gate are preferably given with reference to a diagram as shown in figure 25. The area indicating certain triggering has a lower limit given by the gate-trigger current.

NOTE 1 The values of gate non-trigger voltage and current should be given at maximum rated virtual junction temperature. The values of gate trigger voltage and current should be given at 25 °C and a minimum operating temperature.

NOTE 2 If the characteristics given in figure 25 are different for different quadrants, this should be stated.



I_{GD}	gate non-trigger current	A_1	area of non-triggering
I_{GT}	gate trigger current	A_2	area of uncertain triggering
V_{GD}	gate non-trigger voltage	A_3	area of certain triggering
V_{GT}	gate trigger voltage		

Figure 25 – Forward gate voltage versus forward gate current

6.4.10 Gate-controlled turn-on delay time

Typical and, where appropriate, maximum value(s), under the following specified conditions:

a) gate current amplitude;

b) rise time of gate current, preferably equal to 0,5 µs;

c) minimum duration of the gate pulse, preferably equal to two times the specified delay time of the triac;

d) off-state voltage prior to turn-on, preferably equal to 0,5 times the maximum rated repetitive peak off-state voltage (V_{DRM}) of 6.2.2.

6.4.11 Total power loss

A curve showing the maximum total power loss as a function of r.m.s. sinusoidal on-state current at 50 Hz or 60 Hz.

Where appropriate, the on-state power loss, the turn-on and turn-off loss shall be specified separately.

6.5 Thermal characteristics

6.5.1 Thermal resistance junction to ambient ($R_{th(j-a)}$)

Maximum value for ambient-rated triacs only.

6.5.2 Thermal resistance junction to case ($R_{th(j-c)}$)

Maximum value, for case-rated triacs only.

6.5.3 Thermal resistance case to heatsink ($R_{th(c-h)}$)

Maximum value, for case rated triacs only.

6.5.4 Thermal resistance junction to heatsink ($R_{th(j-h)}$)

Maximum value, for heatsink rated triacs only.

6.5.5 Transient thermal impedance junction to ambient ($Z_{th(j-a)}$)

For ambient-rated triacs only, a curve of $Z_{th(j-a)}$ as a function of the time elapsed following a step change in power loss.

6.5.6 Transient thermal impedance junction to case ($Z_{th(j-c)}$)

For case-rated triacs only, a curve of $Z_{th(j-c)}$ as a function of the time elapsed following a step change in power loss.

6.5.7 Transient thermal impedance junction to heatsink ($Z_{th(j-h)}$)

For heatsink-rated triacs only, a curve of $Z_{th(j-h)}$ as a function of the time elapsed following a step change in power loss.

6.6 Mechanical characteristics and other data

See IEC 60747-1.

6.7 Application data

A statement of the special requirements that are applicable to series or parallel connection of triacs or triac stacks.

The manufacturer should be consulted for detailed recommendations.

7 Essential ratings and characteristics for gate turn-off thyristors (GTO thyristors)

7.1 Thermal conditions

GTO thyristors shall be specified as ambient-rated or case-rated or heatsink-rated devices.

7.1.1 Recommended temperatures

Many of the ratings and characteristics shall be quoted at a temperature of 25 °C and at one other specified temperature. Unless otherwise stated, the one other temperature should be chosen by the manufacturer from the list in IEC 60747-1. In addition, temperatures of –40 °C and +35 °C may be used.

7.1.2 Rating conditions

The ratings given in 7.2 shall be stated under one or more of the following thermal conditions.

A Ambient-rated GTO thyristors

– Natural convection

  At 25 °C and at one higher temperature (see 7.1.1). The cooling fluid and pressure (in the case of a gas) shall be specified.

  Air pressure shall be at least 90 kPa (900 mbar), corresponding to a maximum level of 1 000 m above sea level.

– Forced circulation

  At a temperature taken from the list of recommended temperatures (see 7.1.1).

  The type, pressure and flow rate of the cooling fluid shall be specified.

B Case-rated or heatsink-rated GTO thyristors

At a case or heatsink temperature taken from the list of recommended temperatures (see 7.1.1).

NOTE For small GTO thyristors, the specified reference point at which the temperature is measured may be located on one of the terminals.

7.2 Voltage and current ratings (limiting values)

Unless otherwise stated, the following ratings shall be valid for the whole range of operating conditions as stated for the particular device.

A Anode-cathode voltages

7.2.1 Non-repetitive peak reverse voltage (V_{RSM})

Maximum rated peak value of a non-repetitive reverse voltage pulse.

7.2.2 Repetitive peak reverse voltage (V_{RRM})

Maximum rated peak value of repetitive reverse voltage pulses.

7.2.3 Direct reverse voltage ($V_{R(D)}$) (where appropriate)

Maximum rated value.

7.2.4 Non-repetitive peak off-state voltage (V_{DSM}) (where appropriate)

Maximum rated peak value of a non-repetitive, off-state voltage pulse, under specified gate conditions.

7.2.5 Repetitive peak off-state voltage (V_{DRM})

Maximum rated peak value of repetitive off-state voltage pulses, under specified gate conditions.

7.2.6 Direct off-state voltage ($V_{D(D)}$) (where appropriate)

Maximum rated value.

B Gate voltages

7.2.7 Turn-off gate voltage (V_{RG})

Maximum rated value of the driving voltage in the turn-off gate circuit. The gate voltage will exceed V_{RG} during short time intervals by the transient from the gate-circuit inductance when the (reverse) turn-off gate current begins to fall.

C On-state current

7.2.8 Non-repetitive peak controllable on-state current (I_{TQSM})

Maximum rated value under the following conditions:

a) maximum rated virtual junction temperature;

b) specified reapplied off-state voltage, preferably a half or two-thirds of the maximum rated repetitive peak off-state voltage;

c) specified rate of rise of the reapplied off-state voltage;

d) specified turn-off spike voltage;

e) specified driving voltage in the gate circuit, preferably equal to the maximum rated turn-off gate voltage;

f) specified rate of rise of the turn-off gate current.

7.2.9 Repetitive peak controllable on-state current (I_{TQRM})

Maximum rated value under the following conditions:

a) maximum rated virtual junction temperature is reached at the end of the turn-off procedure;

b) specified reapplied off-state voltage, preferably a half or two-thirds of the maximum rated repetitive peak off-state voltage;

c) specified rate of rise of the reapplied off-state voltage;

d) specified turn-off spike voltage;

e) specified driving voltage in the gate circuit, preferably equal to the maximum rated turn-off gate voltage;

f) specified rate of rise of the turn-off gate current.

7.2.10 RMS on-state current ($I_{T(RMS)}$) (where appropriate)

Maximum rated value under continuous operating conditions.

7.2.11 Short-time and intermittent duty current

The maximum rated on-state current under short-time or intermittent duty may be calculated from the resulting total power loss, the transient thermal impedance and the maximum rated virtual junction temperature using the formulae given in annex A.

7.2.12 Surge on-state current (I_{TSM})

Maximum rated peak values under the following conditions:

a) initial conditions corresponding to the maximum rated virtual junction temperature. In addition, figures corresponding to lower virtual junction temperatures may be given;

b) with no off-state or reverse voltage reapplied after the on-state current loading. In addition, figures valid with specified values of reapplied reverse voltage may be given;

c) for the following waveforms and time periods:

   i) a single 50 Hz or 60 Hz half sine wave,

   ii) for time intervals between 0,1 ms and 10 ms in terms of the maximum rated I^2t value of

$$\int i^2 dt$$

These ratings may be given by means of a curve or by specifies values.

NOTE Although surge on-state current ratings are given for half sine waves, they are, according to experience, also applicable to approximately triangular current waveforms as occur when a sinusoidally rising fault current is interrupted by a current-limiting fuse.

7.2.13 Critical rate of rise of on-state current ($(di_T/dt)_{cr}$)

Maximum rated value under the following conditions:

a) maximum rated virtual junction temperature prior to the current pulse;

b) specified off-state voltage before turn-on, preferably a half or two-thirds of the maximum rated repetitive peak off-state voltage;

c) specified peak value of the on-state current pulse, preferably equal to the maximum rated repetitive peak controllable on-state current, with current wave shape and pulse width specified;

d) specified triggering conditions;

e) specified repetition frequency;

f) specified snubber circuit;

g) test duration (should be longer than the thermal time constant of the device, for example 30 s).

7.3 Other ratings (limiting values)

A Power ratings (limited values)

7.3.1 Peak forward gate power (P_{FGM})

Maximum rated value for a specified pulse width and repetition rate.

B Temperature ratings

7.3.2 Virtual junction temperature (T_{vj})

Maximum rated value.

7.3.3 Storage temperatures (T_{stg})

Minimum and maximum values.

7.3.4 Maximum permissible soldering temperature for GTO thyristors having solder terminals (T_{sld})

For GTO thyristors having solder terminals, the maximum soldering temperature and duration shall be specified.

C Mechanical ratings

7.3.5 Mounting torque (for GTO thyristors having screw connections) (M)

For GTO thyristors having screw connections, the maximum and minimum rated torque values shall be specified.

7.3.6 Clamping force (for disc-type devices) (F)

For GTO thyristors designed for mounting by means of clamps (disc-type devices), the minimum and maximum rated clamping force values and the stiffness of mounting surfaces shall be specified.

7.4 Electrical characteristics

To be specified for 25 °C ambient or case temperature, unless otherwise stated.

7.4.1 On-state voltage (V_T)

Maximum value under the following conditions:

a) specified on-state current, preferably equal to the maximum rated repetitive peak controllable on-state current;

b) at a case or ambient temperature equal to the maximum rated virtual junction temperature. If a defined relationship exists between the values at this temperature and at 25 °C, the value at the latter temperature may be given;

c) specified value of gate current (required to maintain full on-state conduction).

7.4.2 Threshold voltage ($V_{T(TO)}$)

Maximum value at maximum rated virtual junction temperature.

7.4.3 On-state slope resistance (r_T)

Maximum value at maximum rated virtual junction temperature.

7.4.4 Holding current (I_H)

Maximum value at specified off-state voltage, preferably 24 V.

7.4.5 Latching current (I_L)

Maximum value at specified off-state voltage, preferably 24 V and specified triggering conditions, with current waveshape and pulse width specified.

7.4.6 Critical rate of rise of off-state voltage ($(dv_D/dt)_{cr}$)

Maximum value under the following conditions:

a) maximum virtual junction temperature;

b) specified waveform (linear or exponential);

c) specified peak off-state voltage, preferably a half or two-thirds of the maximum rated repetitive peak off-state voltage;

d) specified gate circuit conditions;

e) specified repetition frequency.

7.4.7 Sustaining gate current (I_{FGsus})

Minimum value.

7.4.8 Peak tail current (I_{ZM})

Maximum value under the following conditions:

a) maximum rated junction temperature;

b) on-state current before turn-off equal to the maximum rated repetitive peak controllable on-state current;

c) specified off-state voltage, preferably a half or two-thirds of the maximum rated repetitive peak off-state voltage;

d) specified rate of rise of the reapplied off-state voltage;

e) specified turn-off gate driving voltage, preferably equal to the maximum rated turn-off gate voltage;

f) specified rate of rise of the turn-off gate current.

7.4.9 Gate trigger current (I_{GT}) and gate trigger voltage (V_{GT})

Minimum values under the following conditions:

a) specified low off-state voltage, preferably 24 V;

b) specified maximum source resistance that will provide sufficient on-state current to assure conduction of all cathode islands.

7.4.10 Gate non-trigger current (I_{GD}) and gate non-trigger voltage (V_{GD})

Maximum values under the following conditions:

a) specified off-state voltage, preferably two-thirds of the maximum rated repetitive peak off-state voltage;

b) maximum rated virtual junction temperature;

c) specified gate-bias conditions.

7.4.11 Peak gate turn-off current (I_{RGQM})

Curve showing the minimum value the gate turn-off pulse generator must be capable of supplying as a function of the peak on-state current to turn the thyristor off under the following conditions:

a) maximum rated virtual junction temperature;

b) specified value of the reapplied off-state voltage, preferably a half or two-thirds of the maximum rated repetitive peak off-state voltage;

c) specified rate of rise of the re-applied off-state voltage;

d) specified driving voltage in the gate circuit, preferably equal to the maximum rated turn-off gate voltage;

e) specified rate of rise of the turn-off gate current;

f) repetition rate.

7.4.12 Turn-on energy loss (E_{ON})

Curves showing the maximum turn-on energy loss for one on-state current pulse as a function of the rate of rise of on-state current with the initial off-state voltage as a parameter (excluding the on-state energy dissipation).

NOTE For half sine waves a good approximation of the rate of rise of the on-state current is:

$$\frac{di_T}{dt} = \frac{3\, I_{TM}}{t_p}$$

where I_{TM} is the amplitude, and t_p is the duration of the half-wave.

7.4.13 On-state energy loss (E_T)

Curves showing the maximum on-state energy loss for one on-state current pulse in the steady state, excluding the turn-on and turn-off loss, as a parameter in a diagram of the maximum allowable peak on-state current as a function of the pulse duration

a) for half sine waves,

b) for rectangular current pulses.

7.4.14 Turn-off energy loss (E_Q)

Curves showing the maximum turn-off energy loss for one on-state current pulse as a function of the peak on-state current with the rate of rise of the off-state voltage, the turn-off peak off-state voltage and the turn-off spike voltage as parameters.

NOTE Turn-on, on-state and turn-off power loss values result when the equivalent energy loss values per pulse are multiplied by the repetition frequency.

7.4.15 (Gate-controlled) delay time (t_{gd})

Typical and, where appropriate, maximum value for a specified value of the peak forward gate current.

7.4.16 Turn-off time intervals

The maximum values of the following time intervals shall be given under the following conditions:

a) specified peak on-state current to be turned off, preferably equal to the maximum rated repetitive peak controllable on-state current;

b) specified reapplied off-state voltage, preferably a half or two-thirds of the maximum rated repetitive peak off-state voltage;

c) specified rate of rise of reapplied off-state voltage;

d) specified turn-off spike voltage;

e) specified driving voltage in the gate circuit, preferably equal to the maximum rated turn-off gate voltage;

f) specified rate of rise of the turn-off gate current;

g) maximum rated virtual junction temperature.

7.4.16.1 (Gate-controlled) turn-off time (t_{gq})

Maximum value.

7.4.16.2 (Gate-controlled) turn-off delay time (t_{dq})

Maximum value.

7.4.16.3 (Gate-controlled) fall time (t_{fq})

Maximum value.

7.4.16.4 Tail time (t_z)

Maximum value.

7.5 Thermal characteristics

7.5.1 Thermal resistance junction to ambient ($R_{th(j-a)}$)

Maximum value, for ambient-rated GTO thyristors only.

7.5.2 Thermal resistance junction to case ($R_{th(j-c)}$)

Maximum value, for case-rated GTO thyristors only.

7.5.3 Thermal resistance case to heatsink ($R_{th(j-h)}$)

Maximum value, for heatsink-rated GTO thyristors only.

7.5.4 Transient thermal impedance junction to ambient ($Z_{th(j-a)}$)

For ambient-rated GTO thyristors only, a curve of $Z_{th(j-a)}$ as a function of the time elapsed following a step change in power loss.

7.5.5 Transient thermal impedance junction to case ($Z_{th(j-c)}$)

For case-rated GTO thyristors only, a curve of $Z_{th(j-c)}$ as a function of the time elapsed following a step change in power loss.

7.5.6 Transient thermal impedance junction to heatsink ($Z_{th(j-h)}$)

For heatsink-rated GTO thyristors only, a curve of $Z_{th(j-h)}$ as a function of the time elapsed following a step change in power loss.

7.6 Mechanical characteristics and other data

See IEC 60747-1.

8 Requirements for type tests and routine tests, marking of thyristors

8.1 Type tests

Type tests are carried out on new products on a sample basis in order to determine the electrical and thermal ratings (limiting values) and characteristics that shall be given in the data sheet and to establish the test limits for future routine tests.

Some or all of the type tests may be repeated from time to time on samples drawn from current production or deliveries, so as to confirm that the quality of the product continuously meets the specified requirements.

The minimum type tests to be carried out on reverse-blocking triode thyristors are listed in table 2.

Some of the type tests are destructive.

8.2 Routine tests

Routine tests are carried out on the current production or deliveries normally on a 100 % basis, in order to verify that the ratings (limiting values) and characteristics specified in the data sheet are met by each specimen.

Routine tests may comprise a selection of the devices into groups.

The minimum routine tests to be carried out on reverse-blocking triode thyristors are listed in table 2.

8.3 Measuring and test methods

The measuring and test methods given in clause 9 shall be applied.

For the endurance tests, the methods given in 9.4 shall be applied.

Table 2 – Minimum type and routine tests for reverse-blocking triode thyristors

	Type test	Routine test
Measurements of characteristics		
On-state voltage	x	x
Other static on-state characteristics	x	
Off-state reverse current	x	x
Other static off-state and reverse characteristics	x	
Holding current	x	x[1)]
Latching current	x	x[1)]
Recovered charge, peak reverse recovery current	x	x[1)]
Gate trigger current and voltage	x	x
Gate non-trigger current	x	x[1)]
Circuit-commutated turn-off time	x	x[1)]
Gate-controlled turn-on time	x	x[1)]
Thermal resistance and transient thermal impedance	x	
Verification of ratings		
Critical rate of rise of off-state voltage	x	
Critical rate of rise of on-state current	x	
Surge on-state current	x	
Peak case non-rupture current	x[2)]	
Endurance tests		
High-temperature a.c. reverse bias test	x	
Thermal cycling load test	x	

[1)] Routine test only for devices with specified maximum or minimum values.

[2)] Type test only for devices with a specified maximum value.

8.4 Marking of thyristors

Each thyristor shall be clearly and indelibly marked with the following information:

– manufacturer’s name and identification;
– manufacturer’s or supplier’s type;
– marking to permit the distinction between anode, cathode and gate terminals.

9 Measuring and test methods

Introduction

With few exceptions, indicated in the titles, the measuring and test methods described in this clause apply to reverse blocking triode thyristors. However, many of them are also applicable to other types of thyristors.

As regards their application to reverse blocking triode thyristors, the polarities shown in the circuits are applicable to P-gate thyristors. However, the circuits can be adapted to N-gate thyristors by changing the polarities of the meters and the sources, as well as the anode and cathode terminals.

9.1 Measuring methods for electrical characteristics

9.1.1 General precautions

9.1.1.1 General precautions for d.c. measurements

For measurements of the on-state characteristics of thyristors, the quality of the source of direct current is not considered to be important, provided that the peak-to-peak ripple is less than 10 %.

For measurements of the off-state or reverse characteristics, the peak-to-peak ripple of the voltage source should not exceed 1 % and particular care should be taken to ensure that the voltage ratings of the thyristors are not exceeded due to any voltage transients.

9.1.1.2 General precautions for a.c. measurements

Diodes may be included in source circuits in order to protect the amplifiers in the oscilloscope from unwanted half cycle pulses.

Where low reverse currents are being measured, it may be necessary to take suitable precautions to avoid pick-up, e.g. a screened transformer and suitable earthing. Care should also be taken to avoid parasitic capacitances.

In addition, particular care should be taken to keep residual inductance as low as possible, especially for high-current devices.

9.1.1.3 Temperature conditions

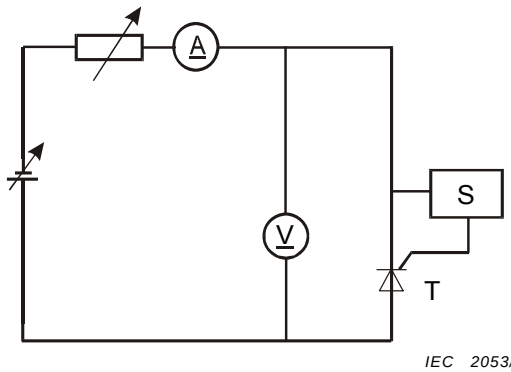
For all measurements of electrical characteristics described below, the conditions of temperature should be specified.

Measurements shall be performed only after thermal equilibrium has been reached.

9.1.2 On-state voltage (V_T)

9.1.2.1 DC method

On-state voltage can be measured using the circuit shown in figure 26. The specified on-state current is set after the thyristor has been switched to the on state and the voltage between the anode and cathode terminals is measured under specified conditions of bias and impedance of the gate circuit.



IEC 2053/2000

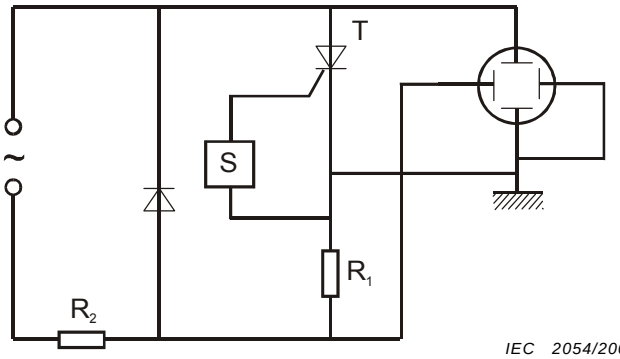
T thyristor under test

S gate-biasing source

Figure 26 – Circuit for measurement of on-state voltage (d.c. method)

9.1.2.2 Oscilloscope method

Figure 27a below shows a circuit for the measurement of instantaneous on-state voltage, using a half sine wave current source under specified conditions of bias and impedance of the gate circuit. The current is applied through the thyristor in the forward direction with the thyristor in the on state. The voltage-current curve is displayed on the oscilloscope as shown in figure 27b.



T thyristor under test
R_2 resistor, low resistance
S gate-biasing source

Figure 27a – Circuit for measurement of on-state voltage (oscilloscope method)

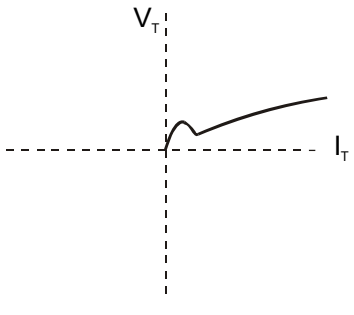


Figure 27b – Graphic representation of on-state voltage versus current characteristic

Figure 27 – Measurement method of instantaneous on-state voltage using oscilloscope

9.1.2.3 Pulse method

Purpose

To measure the on-state voltage of a thyristor under specified conditions, using a pulse method.

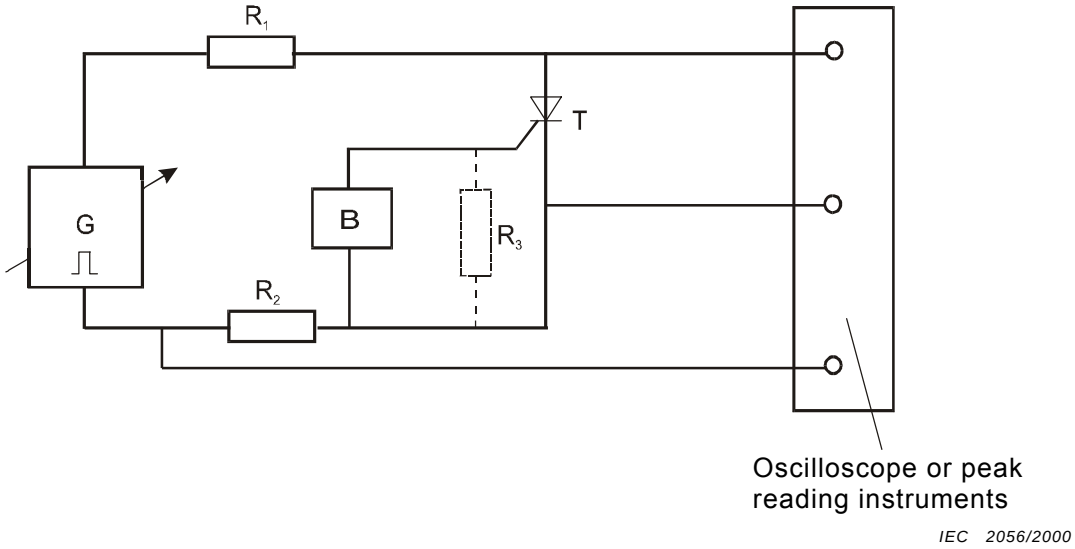


Figure 28 – Circuit diagram for measurement of on-state voltage (pulse method)

Circuit description and requirements

B gate-triggering source

G pulse generator

R_1 protective resistor

R_2 calibrated non-inductive current sensing resistor

T thyristor being measured.

The pulse width and repetition rate of the pulse generator shall be such that negligible internal heating occurs during the measurement.

The duration of the pulse shall be such that the thyristor is fully turned on. With small thyristors and with devices having distributed gate structures, the turn-on spreading time is relatively short, and this condition may be met with pulse widths of 100 µs to 500 µs. With large thyristors having long turn-on spreading times, pulse widths of 1 ms or more may be necessary. If the on-state characteristics for rising current and for falling current are not identical, the characteristic for falling current (i.e. for the fully conducting thyristor) shall be taken. The thyristor may remain in a partly turned-on condition if the current amplitude is not high enough.

Peak reading instruments may be used instead of the oscilloscope, but they must be instruments that allow measurement of the on-state voltage at the time the thyristor is fully turned on.

Precautions to be observed

Care shall be taken not to exceed the rated di/dt of the thyristor being measured.

Measurement procedure

The pulse generator and gate-triggering voltages are initially set to zero.

The specified on-state current is then set by increasing the voltage of the pulse generator; the on-state voltage is measured on the oscilloscope.

Specified conditions

The values of the following conditions shall be stated:

a) peak on-state current;

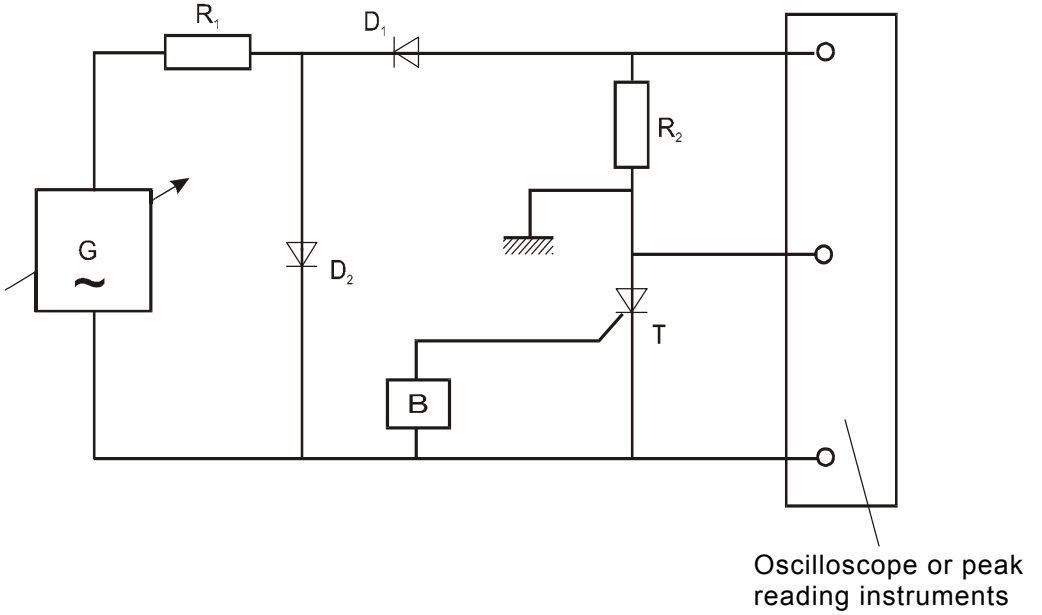
b) ambient, case or reference point temperature;

c) gate-triggering circuit bias conditions, including R_3 as necessary.

9.1.3 Peak reverse current (I_{RM})

Purpose

To measure the peak reverse current of a thyristor at a specified value of repetitive peak reverse voltage under specified conditions.



B	gate circuit
D_1/D_2	diodes to provide negative half cycles, so that only the reverse characteristic of the thyristor is measured
G	alternating voltage source
R_1	protective resistor
R_2	calibrated current sensing resistor
T	thyristor being measured

Figure 29 – Circuit diagram for measuring peak reverse current

Measurement procedure

The repetitive peak reverse voltage across the thyristor, measured on the oscilloscope, is adjusted by means of the alternating voltage source. The peak value of the reverse current through the thyristor is measured on the oscilloscope connected across R_2.

Peak reading instruments may be used instead of the oscilloscope, but they must be instruments that allow measurement of the peak reverse current at the time the reverse voltage reaches its peak value.

Specified conditions

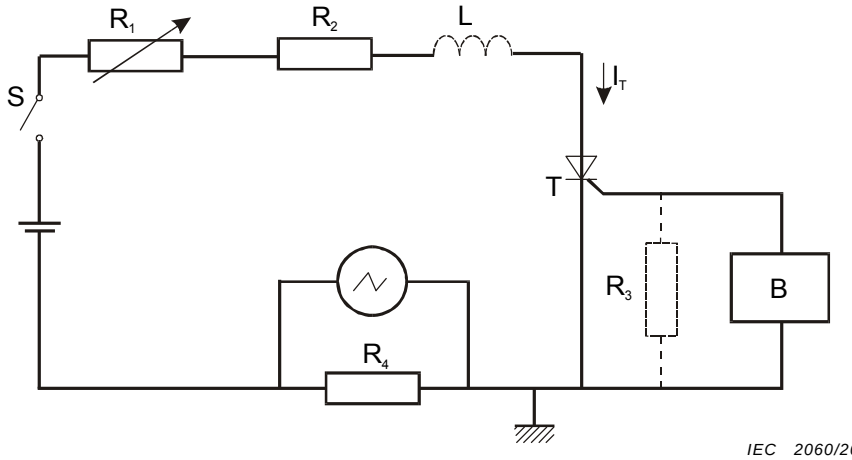
The values of the following conditions shall be stated:

a) repetitive peak reverse voltage;
b) frequency of alternating voltage source;
c) gate bias conditions: source voltage and source resistance or gate-cathode resistor;
d) ambient, case or reference point temperature.

9.1.4 Latching current (I_L)

Purpose

To measure the latching current of a thyristor under specified conditions.



B triggering and gate-bias source

R_2 protective resistor

R_4 calibrated non-inductive current sensing resistor

Figure 30 – Circuit diagram for measuring latching current

Circuit description and requirements

The residual inductance L of the circuit including the d.c. voltage source should be as small as possible.

Measurement procedure

With the resistor R_1 at its maximum value, the thyristor shall not conduct continuously when switch S is closed.

The value of R_1 is then gradually reduced and the principal current allowed to increase until it does not fall at the end of each triggering pulse. The value of the principal current at this point corresponds to the value of the latching current (see figure 31 below).

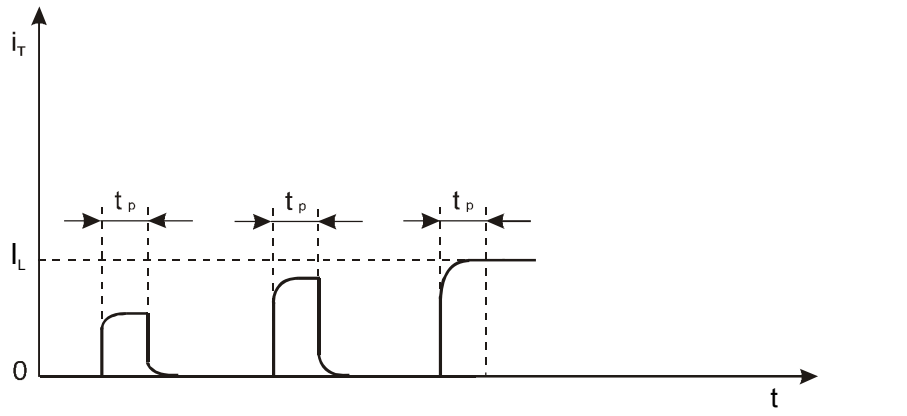


Figure 31 – Waveform of the latching current

The measurement may be repeated to obtain greater accuracy by operating switch S and adjusting the value of R_1 until the critical point at which the latching current is reached is determined accurately.

Specified conditions

The values of the following conditions shall be stated:

a) off-state voltage;

b) gate bias conditions: voltage, polarity and resistance of the gate bias supply, including R_3 as necessary;

c) triggering pulse: rise time, fall time, pulse width, repetition rate, voltage amplitude and resistance of the trigger pulse generator;

d) ambient, case or reference-point temperature.

9.1.5 Holding current (I_H)

Purpose

To measure the holding current of a thyristor under specified conditions.

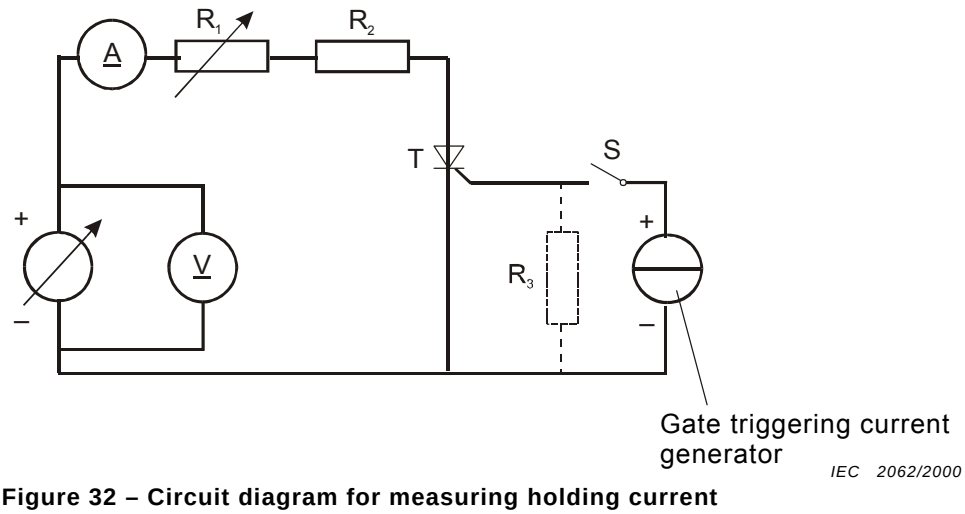


Figure 32 – Circuit diagram for measuring holding current

Circuit description and requirements

Resistor R_2 is a protective resistor. Resistor R_3 shall only be used when specified.

Measurement procedure

The temperature is set to the specified value.

The voltage generator output is increased to obtain the specified value of the off-state voltage V_D.

Switch S is closed and the gate current increased until the thyristor triggers.

R_1 is adjusted so that the on-state current is high enough to ensure that the thyristor is fully turned on.

Switch S is then opened and the on-state current gradually decreased by increasing R_1 until the thyristor turns off.

The value of the on-state current, measured on ammeter A immediately prior to the turn-off point, is the holding current.

Specified conditions

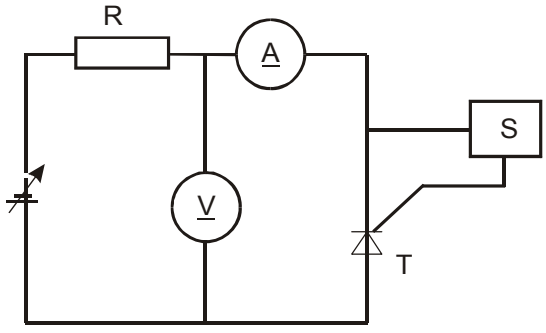
a) ambient, case or reference point temperature (T_a, T_c, T_{ref});
b) (where appropriate) minimum on-state current to ensure that the thyristor is fully turned on;
c) gate circuit resistor (R_3), if required;
d) off-state voltage (V_D).

9.1.6 Off-state current (I_D)

9.1.6.1 DC method

Purpose

To measure the off-state current of a thyristor using d.c. current source.



IEC 2063/2000

S gate biasing source

T thyristor under test

Figure 33 – Circuit diagram for measuring off-state current (d.c. method)

Measurement procedure

The specified forward voltage is applied through the protective resistor R and the off-state current is measured under specified conditions of bias and impedance of the gate circuit.

The protective resistor R shall be sufficiently large to protect the current meter and the device being measured in case the device should switch to the conducting state.

9.1.6.2 Oscilloscope method

Purpose

To measure the peak off-state current of a thyristor at a specified value of repetitive peak off-state voltage under specified conditions.

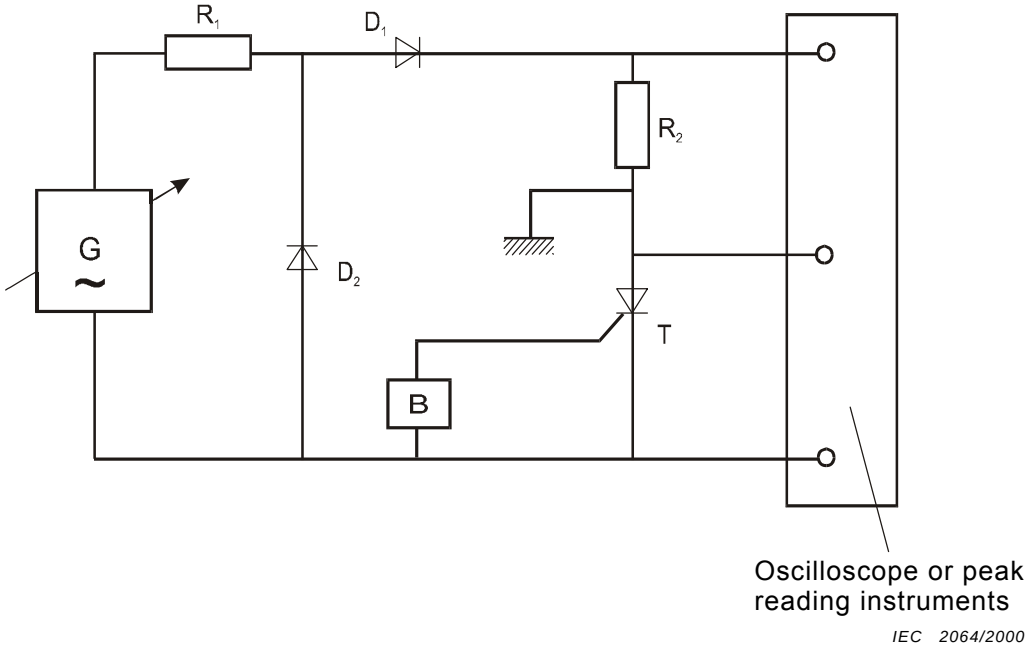


Figure 34 – Circuit diagram for measuring peak off-state current

Circuit description and requirements

B gate circuit

D_1 and D_2 diodes to provide positive half cycles, so that only the off-state characteristic of the thyristor is measured

G alternating voltage source

R_1 protective resistor

R_2 calibrated non-inductive current sensing resistor

T thyristor being measured

Measurement procedure

The repetitive peak off-state voltage across the thyristor, measured on the oscilloscope, is adjusted by means of the alternating voltage source. The peak value of the off-state current through the thyristor is then measured on the oscilloscope connected across R_2.

Peak reading instruments may be used instead of the oscilloscope, but they must be instruments that allow measurement of the peak off-state current at the time the repetitive off-state voltage reaches its peak value.

Specified conditions

The values of the following conditions shall be stated:

a) repetitive peak off-state voltage;
b) frequency of alternating voltage;
c) gate bias conditions: source voltage and source resistance or gate-cathode resistor;
d) ambient, case or reference-point temperature.

9.1.7 Gate trigger current or voltage (I_{GT}), (V_{GT})

Purpose

To measure the gate trigger current and/or voltage of a thyristor under specified conditions.

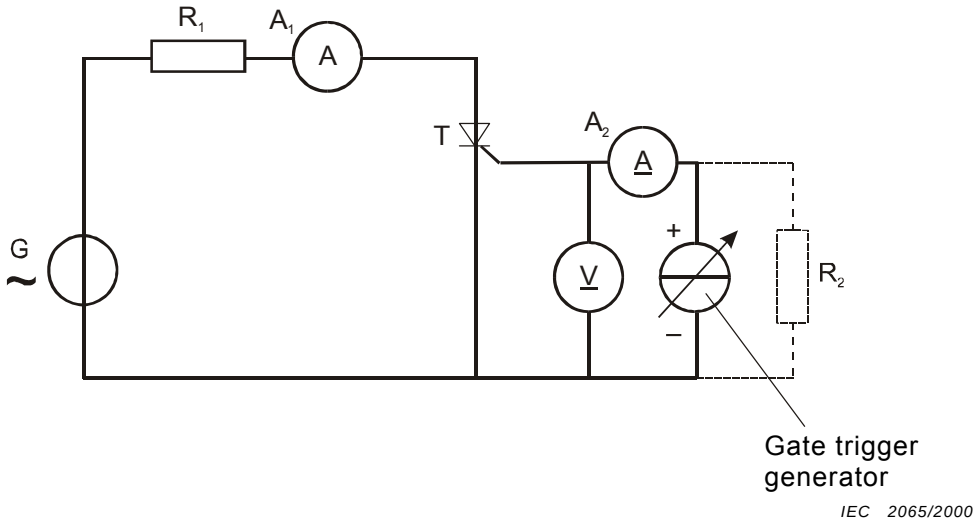


Figure 35 – Circuit diagram for measuring gate trigger current and/or voltage

Circuit description and requirements

Resistor R_1 determines the on-state current which must be high enough to ensure that the thyristor is fully turned on.

The voltage generator G provides a low supply voltage, preferably 12 V or less.

NOTE 1 The alternating voltage generator may be replace by a d.c. generator.

NOTE 2 When measuring very small triggering currents, the voltmeter impedance should be taken into account.

Measurement procedure

The temperature is set to the specified value.

The gate current is gradually increased until the thyristor just triggers and ammeter A_1 indicates an on-state current.

The gate trigger current is the highest recorded value on ammeter A_2 and the gate trigger voltage is the corresponding voltage value measured on voltmeter V.

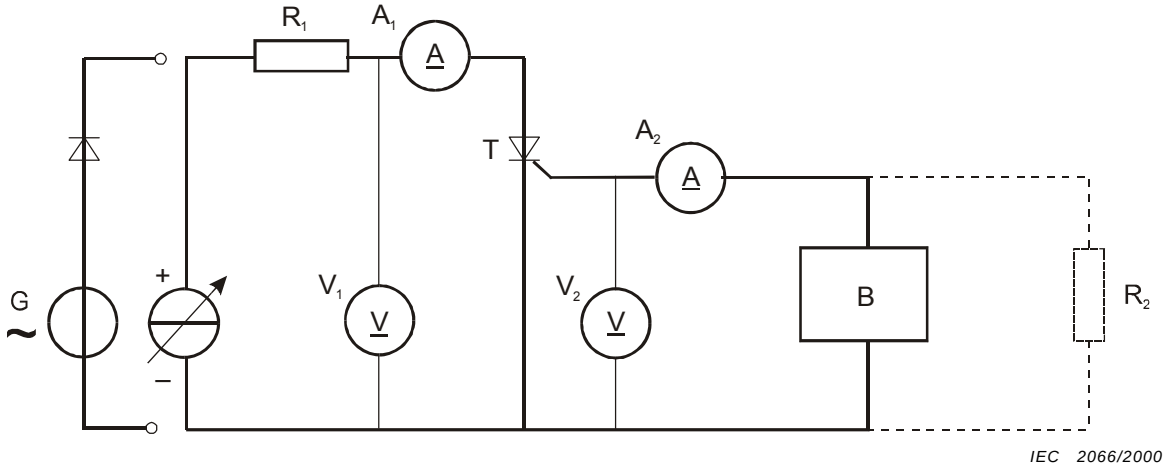
Specified conditions

a) ambient, case or reference-point temperature (T_a, T_c, T_{ref});
b) off-state voltage (to be specified if other than 12 V peak a.c.);
c) frequency of alternating generator (to be specified if greater than 65 Hz);
d) gate circuit resistor R_2 (if required).

9.1.8 Gate non-trigger voltage (V_{GD}) and gate non-trigger current (I_{GD})

Purpose

To verify or to measure the gate non-trigger voltage or the gate non-trigger current of a thyristor under specified conditions.



B DC gate triggering source
T thyristor being measured

Figure 36 – Circuit diagram for measuring gate non-trigger current and/or voltage

Circuit description and requirements

Resistor R_1 is a protective resistor which should be as small as practicable. Resistor R_2 is to be used only when specified.

The d.c. generator may be replaced by an a.c. generator with a diode in series, in which case voltmeter V_1 and ammeter A_1 should be peak reading instruments.

Verification method

The temperature is set to the specified value.

The off-state voltage across the thyristor as measured on voltmeter V_1 is set to the specified value.

The specified gate non-trigger voltage as measured on voltmeter V_2 is applied to the gate of the thyristor. The gate non-trigger voltage is verified if the thyristor has not triggered.

Measuring method

The temperature is set to the specified value.

The off-state voltage across the thyristor as measured on voltmeter V_1 is set to the specified value.

The gate voltage is gradually increased until the thyristor triggers and the on-state current flows through ammeter A_1.

The value of the gate voltage immediately prior to triggering, as measured on voltmeter V_2, is the gate non-trigger voltage.

The value of the gate current immediately prior to triggering as measured on ammeter A_2 is the gate non-trigger current.

Specified conditions

a) ambient, case or reference-point temperature (T_a, T_c, T_{ref});

b) off-state voltage V_D (or V_{DM});

c) gate circuit resistance R_2 (if required);

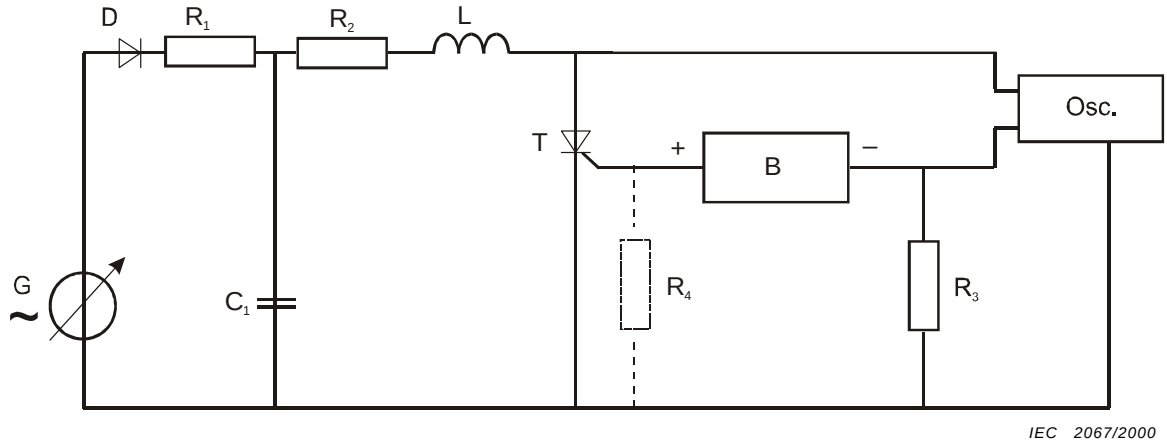
d) gate non-trigger voltage (V_{GD}) (for verification method only);

e) gate non-trigger current.

9.1.9 Gate controlled delay time (t_d) and turn-on time (t_{gt})

Purpose

To measure the gate controlled delay time and turn-on time (delay time + rise time) of a thyristor under specified conditions.



T thyristor being measured
B gate triggering source
Osc. dual-beam oscilloscope

Figure 37 – Circuit diagram for measuring the gate controlled delay time and turn-on time

Circuit description and requirements

To obtain the required rate of rise of on-state current of a thyristor under test T, R_2, C_1, and L shall be such that their values are approximately related to the test voltage V_D, current magnitude I_{TM} and time t_1 as follows:

$$C_1 = 5{,}6 \frac{I_{TM} \cdot t_1}{V_D}$$

$$L = 1{,}7 \frac{V_D \cdot t_1}{I_{TM}}$$

$$R_2 = 0{,}55 \frac{V_D}{I_{TM}}$$

$$di/dt = 0{,}5 \frac{I_{TM}}{t_1}$$

where t_1 is the rise time of the on-state current needed to reach 0,5 I_{TM} as shown in the figure below.

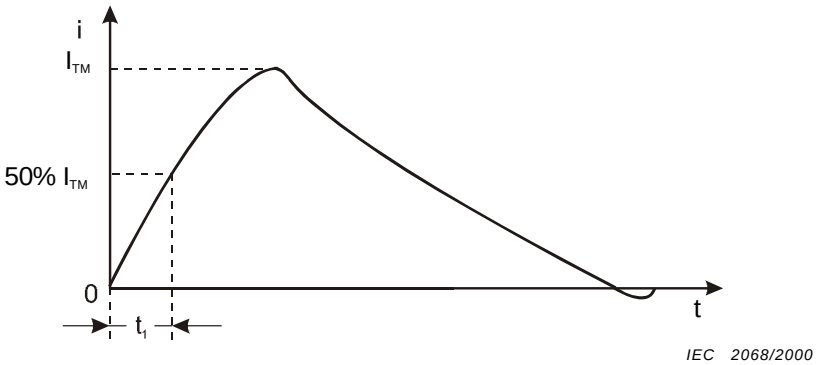


Figure 38 – On-state current waveform of a thyristor

R_1 is a resistor protecting the diode D when the capacitor C_1 is being charged.

Resistor R_4 is only to be used when specified.

Capacitor C_1 is charged on one half cycle of the supply voltage through D and R_1. On the next half cycle, the gate-trigger pulse generator shall be synchronized so that the gate-trigger pulse is applied while the charging supply is negative.

One input to the oscilloscope is the voltage across the thyristor and the other input is the voltage across the non-inductive calibrated resistor R_3.

Precautions to be observed

The half amplitude pulse width shall be large enough not to influence the measurement result (preferably greater than or equal to 10 µs).

Measurement procedure

The temperature is set to the specified value.

The gate triggering source is switched on.

The off-state voltage measured on the oscilloscope is increased to the specified value.

The delay and rise times can be observed by means of a dual-channel oscilloscope (see figure 39).

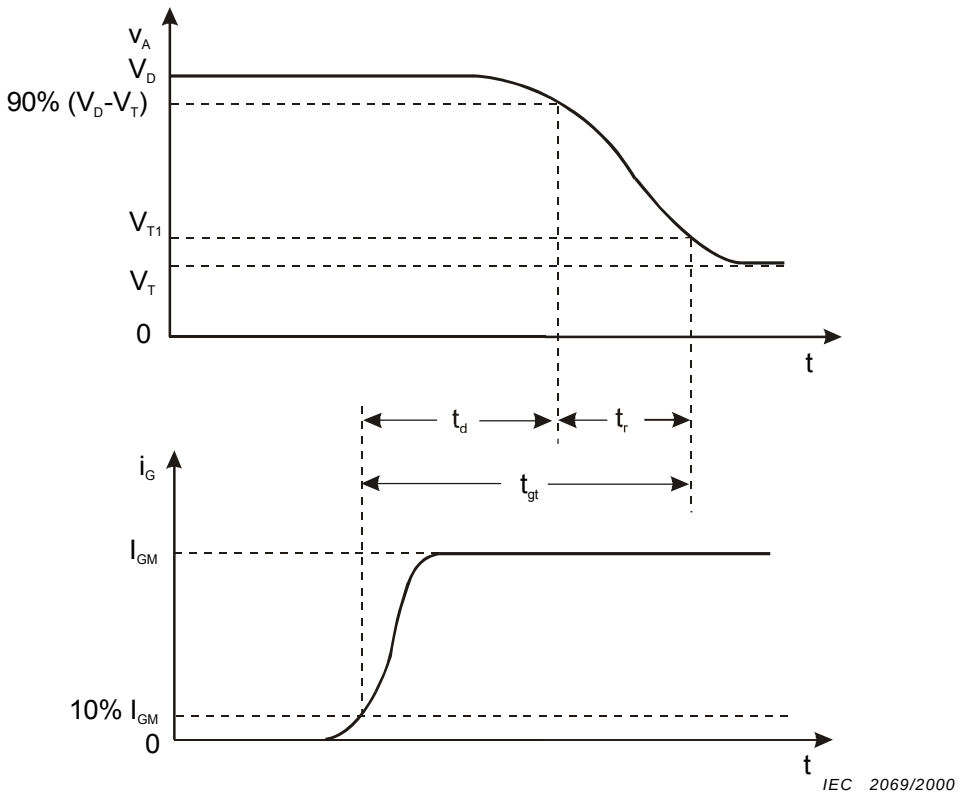


Figure 39 – Off-state voltage and current waveform of a thyristor

Specified conditions

a) ambient, case or reference point temperature (T_a, T_c, T_{ref});

b) gate current (I_{GM});

c) rise time, duration and repetition rate of the gate pulse;

d) off-state voltage just prior to applying the gate current (V_D);

e) peak anode current (I_{TM});

f) gate circuit resistance R_4 (if required);

g) di/dt;

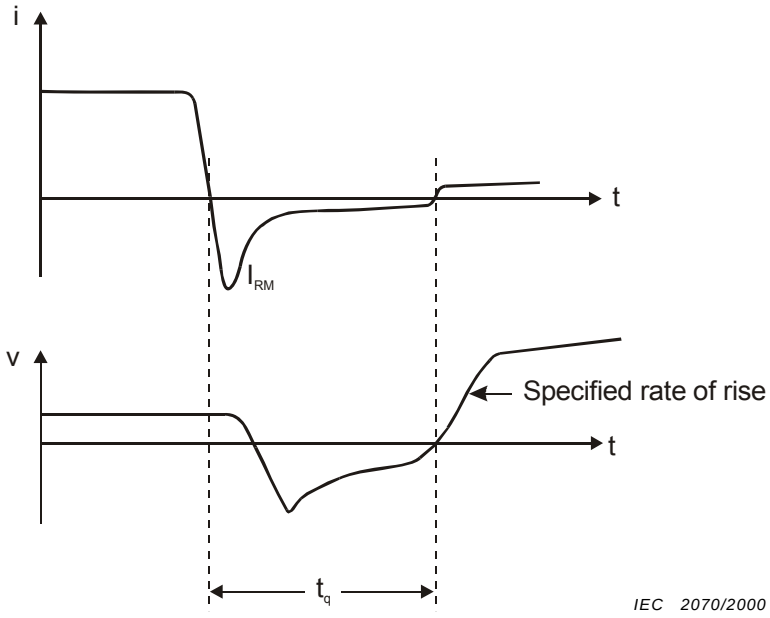
h) turn-on voltage (V_{T1}).

9.1.10 Circuit commutated turn-off time (t_q)

Purpose

To measure the circuit commutated turn-off time of a thyristor under specified conditions.

NOTE It is measured from the instant when the principal current has fallen to zero and the time when the thyristor is capable of blocking the off-state voltage without switching to the on state.

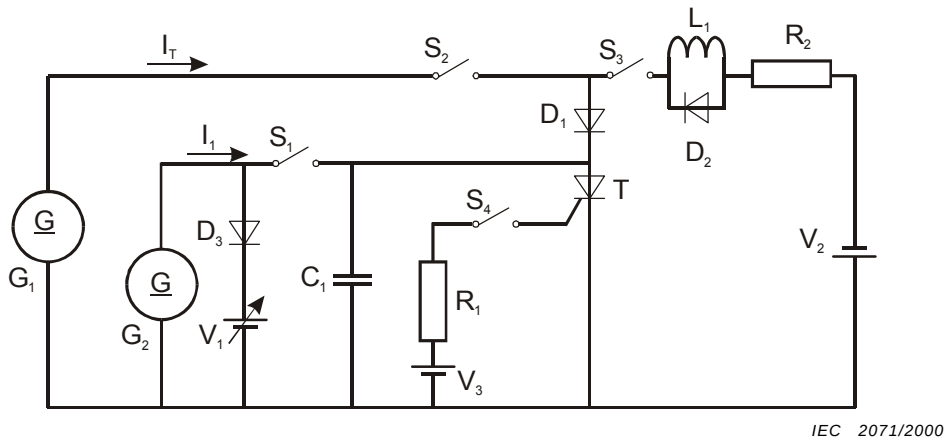


i thyristor anode current
v thyristor anode voltage
I_{RM} peak reverse current

Figure 40 – Thyristor switching waveforms

Operating principle

The basic circuit diagram in figure 41 indicates the operating principles of a circuit used to generate the waveforms shown in figure 40. For convenience, the circuit uses current generators and ideal switches.



G_1 (on-state) constant current generator
G_2 (variable rate of rise) constant current generator
T thyristor under test
V_2 reverse voltage supply

Figure 41 – Diagram of basic circuit

The operation of the circuit is as follows:

a) switches S_2 and S_4 are closed simultaneously causing the thyristor to switch to the on state and conduct the specified current I_T. Switch S_4 is then opened and the trigger circuit disconnected from the thyristor, the on-state current being unaffected;

b) after the specified conduction time, switch S_3 is closed and a reverse voltage of specified amplitude is applied across the thyristor to cause current reversal through the thyristor with specified rate of change;

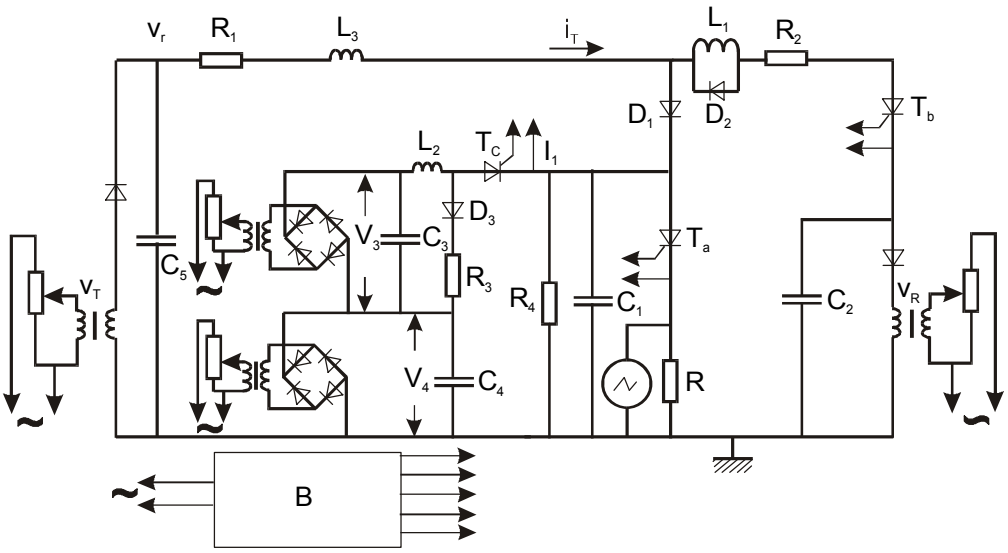
c) switch S_1 is closed so that blocking voltage of specified amplitude and rate of change is applied across the thyristor to determine whether the thyristor is capable of blocking the off-state voltage without switching to the on-state. The switching sequence (S_3 to S_1) is repeated, using successively shorter time intervals, until the time interval is just long enough to allow the off-state voltage to be applied without breakover.

In the circuit diode D_1 shall have a reverse recovery time longer than the reverse recovery time of the thyristor, so that the full reverse voltage cycle appears across the thyristor. Diode D_2 is used to prevent a commutation voltage transient when the thyristor begins to recover its reverse blocking capability.

Diode D_3 is used in conjunction with the voltage V_1 to limit the blocking voltage. Inductor L_1 and resistor R_2 are used to determine the rate of current change during switching from the on state. The current I_1 completes the reverse recovery of diode D_1 and then charges capacitor C_1 linearly with time at a rate equal to I_1/C_1, producing the required rate of rise of blocking voltage at the end of the switching cycle.

9.1.10.1 First method

The measurement is usually made in a circuit operating on a repetitive basis at commercial supply frequency, so that a continuous oscilloscope display is possible. Figure 42 shows an example of such a circuit.



B gate trigger circuit
T_a thyristor being measured
v_T on-state current source
v_r variable rate of rise supply
v_R reverse voltage source

Figure 42 – Practical circuit

Circuit description and requirements

The on-state current I_T is obtained from the charge in capacitor C_5 which is charged by means of an adjustable half wave rectified supply. The time constant C_5 R_1 shall be sufficiently large so that the specified on-state current is essentially constant over the specified conduction period. L_3 limits the rate of rise of on-state current.

The circuit used in figure 42 to generate the blocking voltage differs from that shown in the basic circuit in figure 41. When thyristor T_c is triggered, diode D_3 is reverse biased (because of the voltage on capacitor C_4) causing the current through inductor L_2 to be diverted through T_c to charge capacitor C_1 at a linear rate. The inductance of L_2 shall be large enough to maintain constant current until capacitor C_1 charges to a voltage equal to the sum of voltages V_3 and V_4.

At this point, diode D_3 starts to conduct and clamps the off-state voltage applied to the thyristor being measured. Resistor R_4 is used to discharge capacitor C_1 during the conduction period before the next switching cycle. Resistor R_3 serves to control the value of the constant current through L_2 and D_3.

In addition, the following considerations are applicable:

a) the time constant R_1C_5 shall be large enough to maintain an essentially constant current during the conduction period. For test currents above 100 A, a properly designed lumped constant transmission line and a reduced repetition rate may result in a more practical source of conduction current;

b) thyristor T_b does not turn off until the charges on C_2 and C_5 reach equilibrium. This results in considerable power loss in R_1 and R_2. This loss can be considerably reduced by adding additional circuitry for turning off thyristor T_b following the triggering of thyristor T_c or by reducing the pulse repetition rate;

c) resistor R_4 provides a discharge path for capacitor C_1. The current drawn by R_4 shall be less than the holding current of thyristor T_c so that it may turn off after C_1 becomes charged;

d) effects of distributed capacitance in L_2, reverse recovery of diodes D_1 and D_3 and wiring inductance may cause undesirable oscillations in the re-applied forward voltage waveform. These effects can be minimized by good design practices including the use of suitable damping resistances (not included in figure 42);

e) good design practice shall be used to avoid exceeding ratings of the components selected.

Measurement procedure

The gate trigger generator is synchronized with the supply frequency and provides trigger pulses on the half cycle following the charging of capacitors C_5 and C_2. Trigger pulses are applied to the thyristor under test T_a and to thyristors T_b and T_c, in that order, to perform the switching functions of switches S_4, S_3, and S_1 of figure 41.

The conduction period is ended by the gate pulse which triggers thyristor T_b, allowing the reverse voltage of capacitor C_2 to be applied through resistor R_2, inductor L_1 and diode D_1 across the thyristor being measured, the functions and requirements of R_2, L_1 and D_1 being as described for the basic circuit.

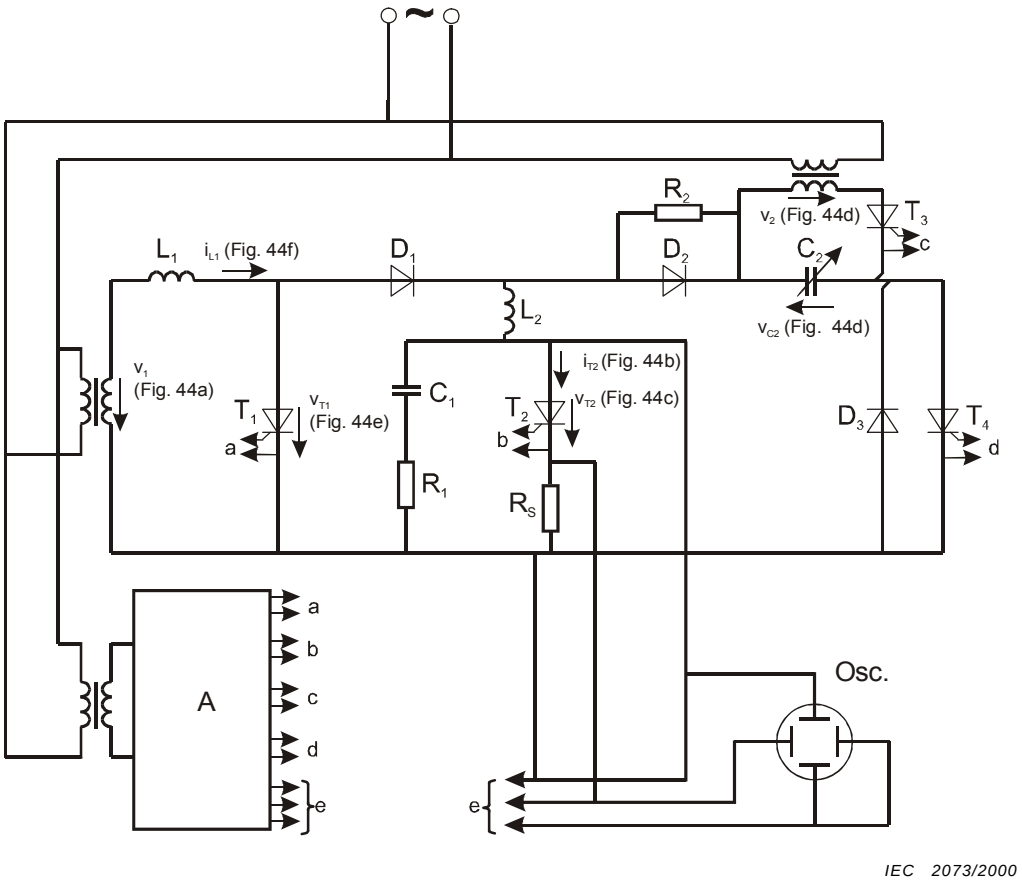
The turn-off time interval is ended by the gate pulse which triggers thyristor T_c.

9.1.10.2 Alternative method

An alternative method to measure the circuit commutated turn-off time, especially for high current devices, is shown in figure 43. The voltage and current waveforms in the measuring circuit are given in figures 44a to 44f.

Circuit description and requirements

The operation of the circuit in figure 43 is as follows:



A	control unit
T_2	thyristor being measured
Osc.	double beam oscilloscope
v_1	forward supply
v_2	reverse voltage supply

Figure 43 – Measurement circuit

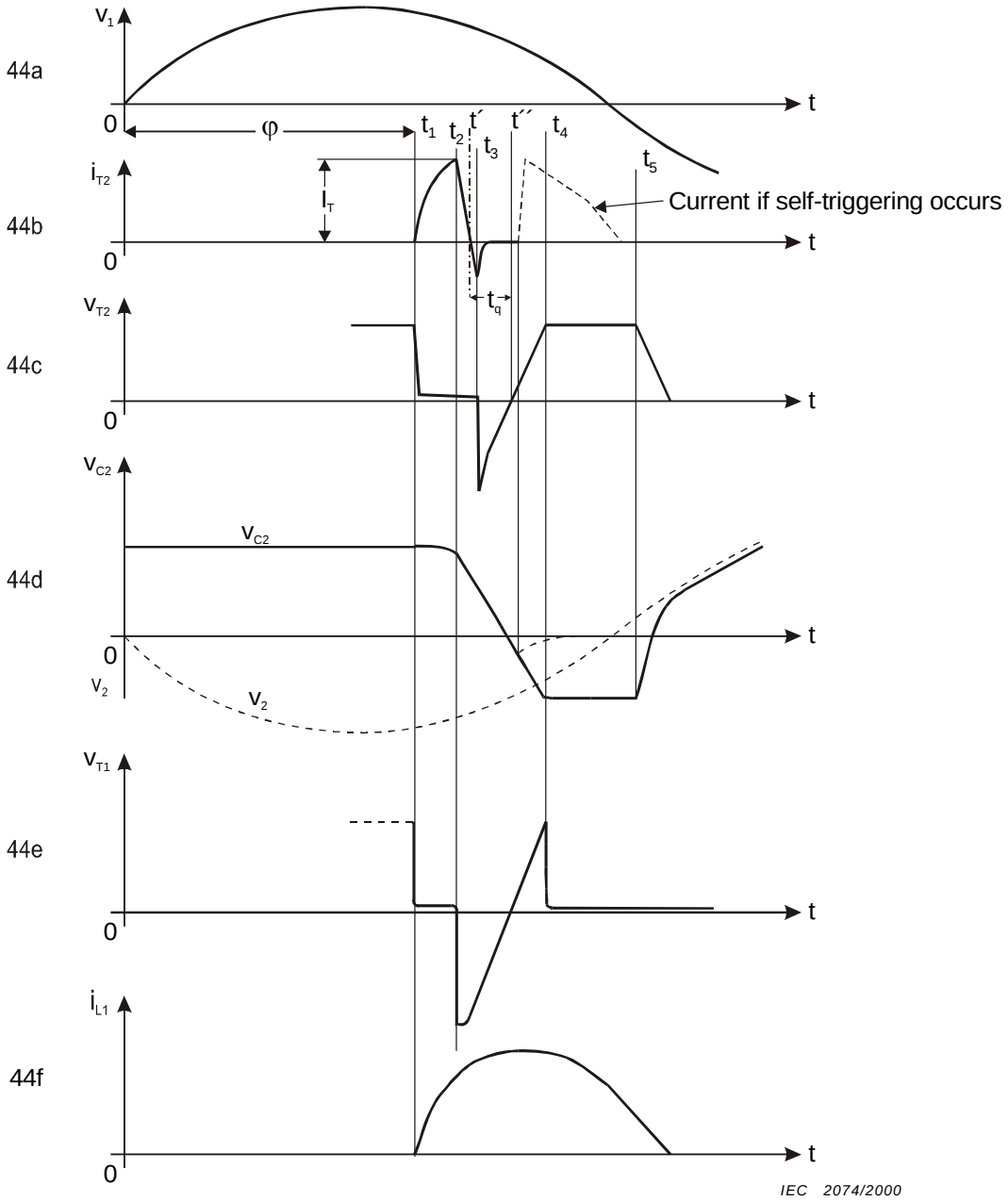


Figure 44 – Voltage and current waveforms

During the negative half cycle of the voltage v_1, the capacitor C_2 is charged by the positive half cycle of the auxiliary voltage v_2 to approximately the peak value of v_2 via thyristor T_3 which, at time t_5 (see figures above), is switched on by the control unit. Before the start of the measuring process, C_2 shall be completely charged and thyristor T_3 shall be completely cut-off.

The measuring process starts when the thyristor being measured T_2 is switched on by the control unit at time t_1 (see figures 44 a-f), i.e. immediately after the supply voltage v_1 reaches its peak value (control angle φ between 100° and 110°). The current i_{T2} through the thyristor being measured (see figure 44b) increases with an initial slope determined by the inductances L_1 and L_2. The circuit for this current flow consists of the transformer, L_1, D_1, L_2, T_2 and back

to the transformer. At time t_2 (adjustable by the control unit), the current i_{T2} reaches the value I_T specified for the thyristor being measured and, at the same time, thyristor T_4 is switched on by the control unit. Thus, the capacitor C_2 discharges through the circuit consisting of thyristor T_4, measuring resistor R_S, the thyristor being measured T_2, inductance L_2 and diode D_2, until at time t_3 (see figure 44b) thyristor T_2 is cut-off. The rate of fall of i_{T2} is determined mainly by the value of L_2. The residual voltage of capacitor C_2 acts at this time as reverse voltage for the thyristor being measured. However, due to the hole storage effect, the voltage across T_2 is momentarily larger than the voltage across capacitor C_2. The resulting voltage transient is limited in amplitude by the series connection of capacitor C_1 and resistor R_1 shunting the thyristor being measured T_2.

After time t_3 the capacitor C_2 is charged with opposite polarity through the circuit consisting of thyristor T_4, voltage source v_1, inductance L_1 and diodes D_1 and D_2. The almost linear rise of voltage across capacitor C_2 (and therefore also across the thyristor being measured) is mainly due to the magnetic energy stored in inductance L_1 (see figures 44c and 44d). If the voltage across the thyristor under test T_2 reaches the specified blocking voltage (e.g. two-thirds of the repetitive peak off-state voltage), the thyristor T_1 is switched on at time t_4.

This requires an appropriate design of the control unit. The current flowing through inductance L_1 (and until that moment also through capacitor C_2) is taken over by thyristor T_1. The charging of C_2 is thus ended (see figures 44d and 44e). The voltage of capacitor C_2 acts via the resistor-diode combination D_2, R_2 and diode D_3 as an almost constant blocking voltage across the thyristor under test T_2 until at time t_5 (see figure 44d), when charging thyristor T_3 is again switched on by the control unit. The capacitor C_2 is then charged in the opposite direction from the voltage source v_2 for the next measuring cycle.

If the thyristor under test does not withstand the applied blocking voltage and therefore switches on, the capacitor C_2 discharges through the circuit consisting of current limiting resistor R_2, thyristor under test T_2 and diode D_3. The resistor R_2 is shunted by a diode D_2, in order to avoid an unacceptable damping of the charging circuit of capacitor C_2.

NOTE An exponential test waveform can be used as long as the proper correlating factor is established with the standard test method.

It should be noted that the energy stored in inductance L_2, as well as the charge stored in capacitor C_1, may cause an increase of the turn-off time by increasing the charge dissipated while the thyristor under test is switching off.

Components requirements

The inductances L_1 and L_2 and the capacitor C_2 are determined by the following formulae:

$$C_2 \approx I_T \frac{t_q}{V_2}$$

$$L_1 > V_2 \frac{t_q}{0{,}05 \cdot I_T}$$

$$L_2 = V_2 \frac{\Delta t_f}{I_T}$$

where

t_q is the turn-off time of the thyristor being measured;

I_T is the specified current through the thyristor under test before applying the off-state voltage (see figure 44b);

V_2 is the specified peak reverse voltage;

$\Delta t_f = t_3 – t_2$ is the specified time of fall of the on-state current (see figure 44b).

When specifying the circuit components, it should be taken into consideration that the thyristors T_1 and T_4 together with the diodes D_1, D_2 and D_3 shall have rated values of current and voltage at least equal to those of the thyristor under test.

Measurement procedure

The measurement of the circuit commutated turn-off time is made in the following manner:

By decreasing the value of capacitance C_2, the rate of rise of the voltage v_{T2} is increased and the time interval t″ – t' shortened until the thyristor under test is switched on. The circuit commutated turn-off time can then be determined on the oscilloscope as the minimum time difference for which no switch-on occurs between the instants at which the values of current i_{T2} and of the voltage v_{T2} pass through zero (respectively t' and t") (see figures 44b and 44c).

The circuit commutated turn-off time may also be obtained using a single trace oscilloscope by measuring only the time difference between successive instants at which the voltage v_{T2} passes through zero (t″ – t_3). The time difference between the initial instants when v_{T2} passes through zero and the instants at which i_{T2} passes through zero (t_3 – t′) can be determined either by calculation or by measuring average values.

The circuit commutated turn-off time is then the sum of these two time differences.

This method has the advantage that the current measuring resistor R_S may be omitted.

9.1.10.3 Specified conditions (for both methods)

The following conditions shall be specified:

a) the magnitude and rate of fall of the on-state current;

b) the magnitude of the reverse voltage applied during the turn-off interval;

c) the magnitude and rate of rise of the re-applied off-state voltage;

d) the gate bias conditions;

e) ambient, case or reference-point temperature.

9.1.11 Critical rate of rise of off-state voltage (dv/dt)

Purpose

To verify that, at the specified minimum rate of rise of off-state voltage, the thyristor remains in the off state.

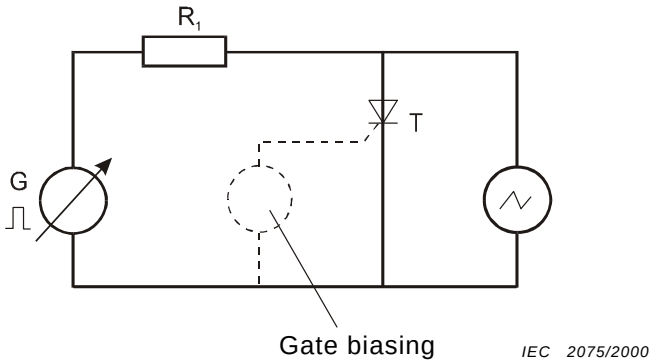


Figure 45 – Circuit diagram for measuring critical rate of rise of off-state voltage

Circuit description and requirements

One of the following two methods of making this measurement should be specified:

9.1.11.1 Method 1 (linear rate of rise)

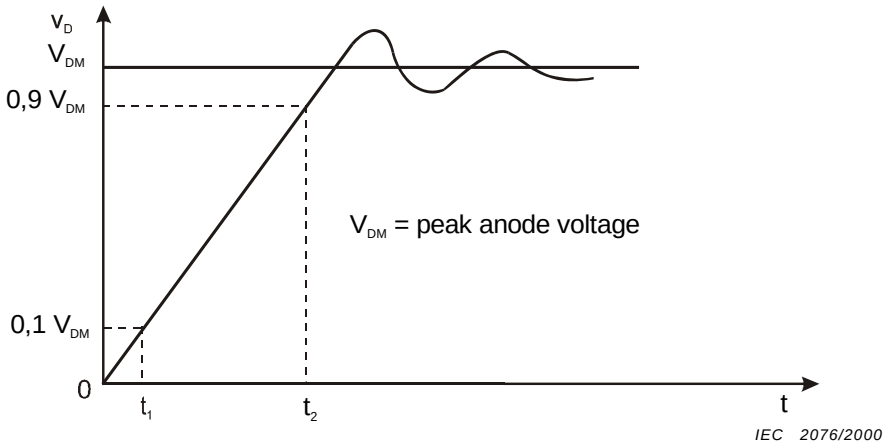


Figure 46 – Waveform

The pulse generator provides a linear waveform of specified amplitude and adjustable linear rate of rise of voltage as shown in figure 46. The straight line connecting the 10 % and 90 % V_{DM} points shall have the specified slope of the critical rate of rise of off-state voltage.

The following conditions shall be met:

– the instantaneous anode voltage between 10 % and 90 % V_{DM} shall not vary by more than 10 % V_{DM} from the straight line connecting the 10 % and 90 % V_{DM} points;

– the instantaneous slope of the anode voltage between 10 % and 90 % V_{DM} shall not vary by more than $\pm$100 % from the slope of the line connecting the 10 % and 90 % V_{DM} points;

– the slope of the straight line connecting the 5 % and 10 % V_{DM} points shall not be less than 75 % of the slope of the straight line connecting the 10 % and 90 % V_{DM} points;

– the peak of the anode voltage overshoot shall not exceed 10 % of V_{DM} unless otherwise specified.

The test may be made repetitively, provided that the pulse width is at least five times the total pulse rise time, and that any anode capacitance is discharged between each pulse.

Resistor R_1 is a protective resistor.

The gate biasing circuit is only to be used when specified.

9.1.11.2 Method 2 (exponential rate of rise)

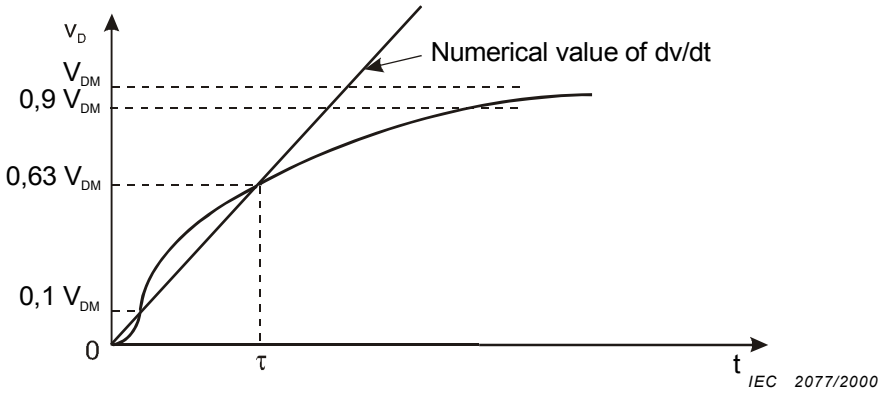


Figure 47 – Measurement circuit for exponential rate of rise

Circuit description and requirements

The pulse generator provides an exponential waveform of specified amplitude and adjustable exponential rate of rise of voltage as shown in figure 47.

The theoretical exponential curve which passes through the actual curve at 0,1 V_{DM} and 0,63 V_{DM} shall have a time constant τ where

$$\tau = \frac{0{,}63\,V_{DM}}{dv/dt}$$

Between 0,1 V_{DM} and 0,9 V_{DM} the voltage shall not differ by more than 5 % V_{DM} from the theoretical exponential.

The test may be made repetitively provided that the pulse duration is at least ten times the time constant τ and that any anode-cathode capacitance is discharged between each pulse.

Resistor R_1 is a protective resistor.

The gate biasing circuit is only to be used when specified.

Measurement procedure (for both methods)

The temperature is set to the specified value.

The amplitude of the voltage from the pulse generator is increased to the specified value as shown on the oscilloscope.

The rate of rise of the voltage from the pulse generator is adjusted to the specified value as shown on the oscilloscope.

The voltage waveform across the thyristor is examined on the oscilloscope.

The test is verified if the thyristor remains in the off state.

Specified conditions (for both methods)

a) ambient, case or reference-point temperature (T_a, T_c, T_{ref});

b) critical rate of rise of voltage dv/dt (specify linear or exponential method);

c) peak off-state voltage (V_{DM});

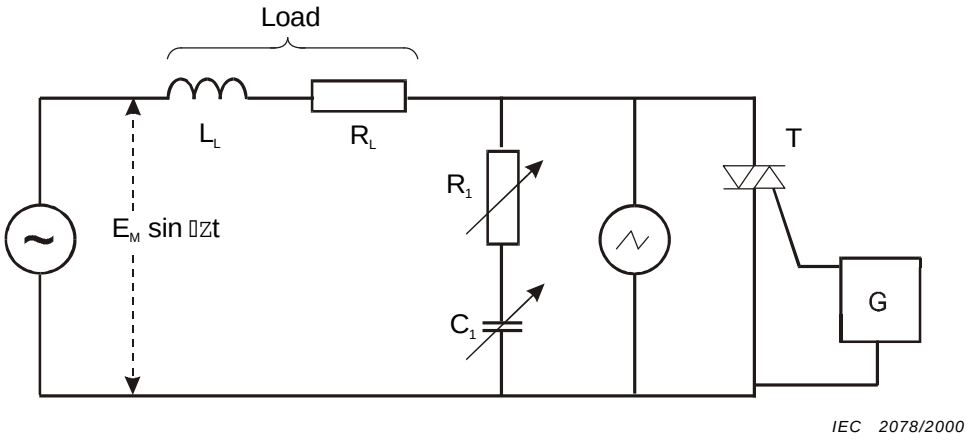
d) gate biasing circuit (if required).

9.1.12 Critical rate of rise of commutating voltage of triacs dv/dt (com)

9.1.12.1 First method: low-current triacs

Purpose

To verify that the triac is able to withstand the rate of rise of commutating voltage without loss of control; this applies to bi-directional thyristors for both polarities of applied voltage.



T triac under measurement

G gate triggering source

Figure 48 – Measurement circuit for critical rate of rise of commutating voltage

Circuit description and requirements

The power source for the measurement circuit is a 50 Hz or 60 Hz single-phase sine wave supply.

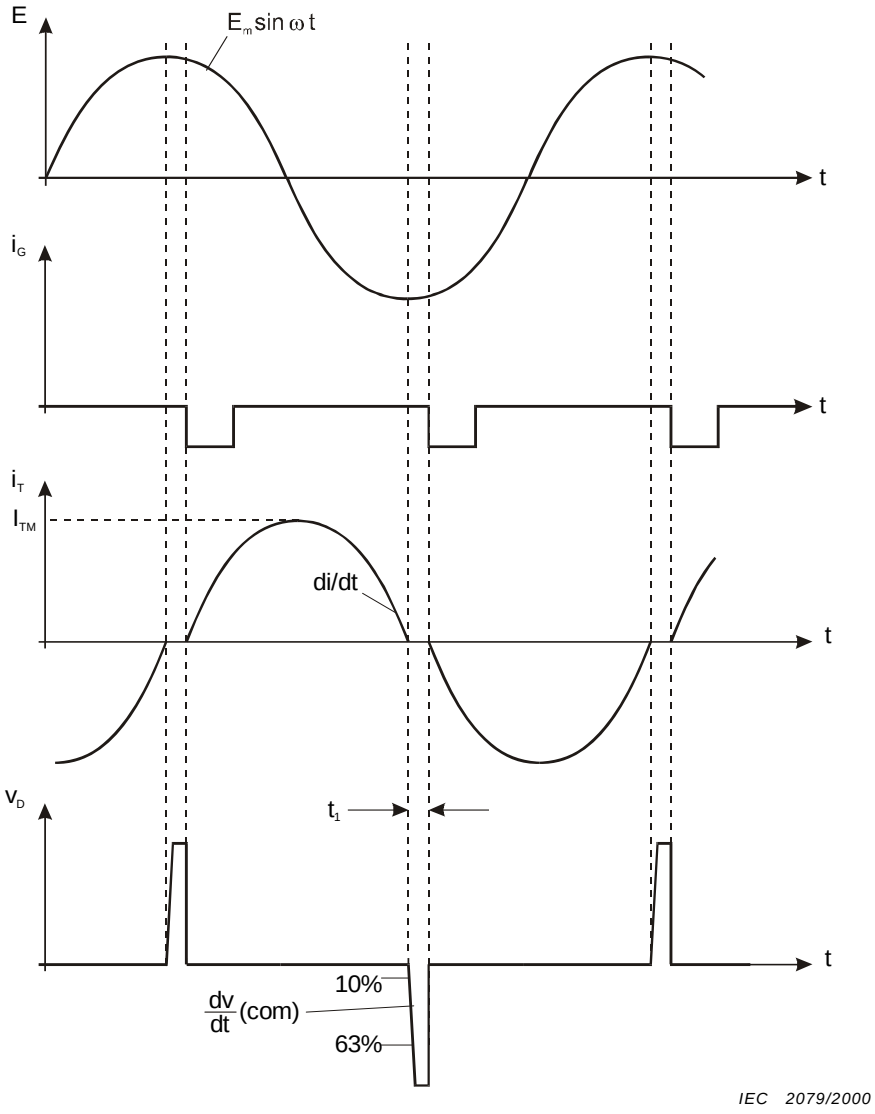
The X/R ratio for the entire measurement circuit shall be greater than or equal to 10 so that the supply voltage and current are essentially in quadrature.

Measurement procedure

The rate of rise of the applied commutating voltage (off-state voltage of the device under measurement) is essentially exponential and is varied by the setting of R_1 and C_1. The oscilloscope connected across the device under measurement is used to examine the waveform of this voltage and so to ensure that the device has not triggered due to excessive dv/dt.

The numerical value assigned to the dv/dt of the exponential voltage waveform is defined as the slope of the straight line connecting the 10 % and 63 % points on the measurement voltage waveform. The 10 % voltage point is used instead of zero because of the difficulty in determining the time point at which zero voltage occurs. The voltage overshoot should be limited to 10 % of the specified peak value of the measurement voltage.

The current and voltage waveforms are shown in figure 49.



t_1: off-state voltage duration

Figure 49 – Waveforms

The triac under measurement passes the test if, after zero-crossing of i_T, v_D rises to V_{DM} and does not drop back towards zero during the specified off-state voltage duration (t_1).

In this method of measurement, the rate of reversal of current (di/dt) is limited by the circuit. Hence, for triacs with very fast switching capability, the device may sustain the off state even when R_1 and C_1 are removed. In this case, the dv/dt of the applied voltage waveform is determined by the capacitance of the triac and the distributed capacitance of other circuit components, particularly the inductor.

Specified conditions

These conditions apply for each half cycle of the test voltage and current:

a) frequency of single-phase sinusoidal a.c. supply (50 Hz or 60 Hz);

b) peak on-state current ($I_{TM} \approx \frac{E_M}{Z_L}$);

c) on-state current duration (90 % of half cycle recommended);

d) rate of reversal of on-state current (di/dt) (the slope of the line connecting the 50 % and 0 % I_{TM} points; di/dt ≈ 2 π f I_{TM});

e) peak off-state voltage ($V_{DM} \approx E_M$);

f) off-state voltage duration (200 µs minimum recommended);

g) gate bias conditions (between current pulses):

gate source voltage,

gate source resistance, or

gate bias resistance;

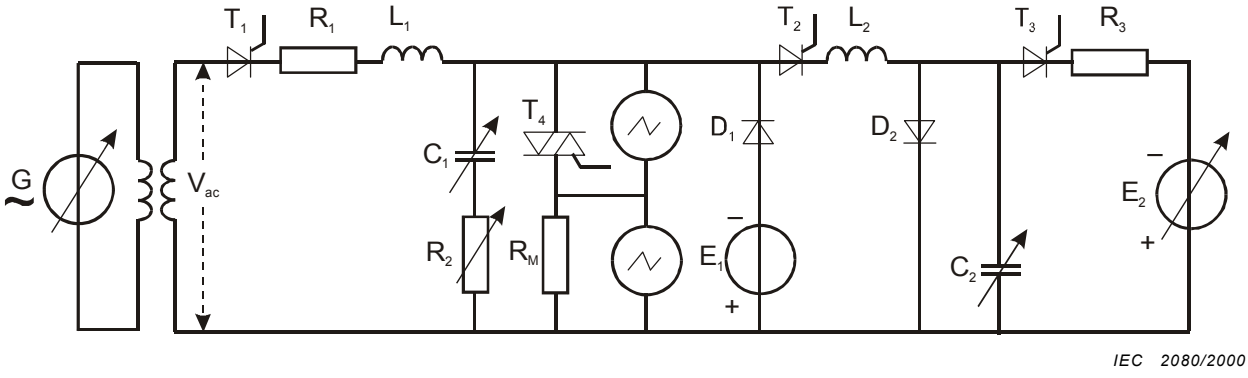
h) ambient, case or reference point temperature.

9.1.12.2 Second method: high-current triacs with high or low rate of decay of on-state current

Purpose

To measure the “critical rate of rise of commutating voltage” of high-current triacs over a large range of values, both under high and low rates of decay of on-state current.

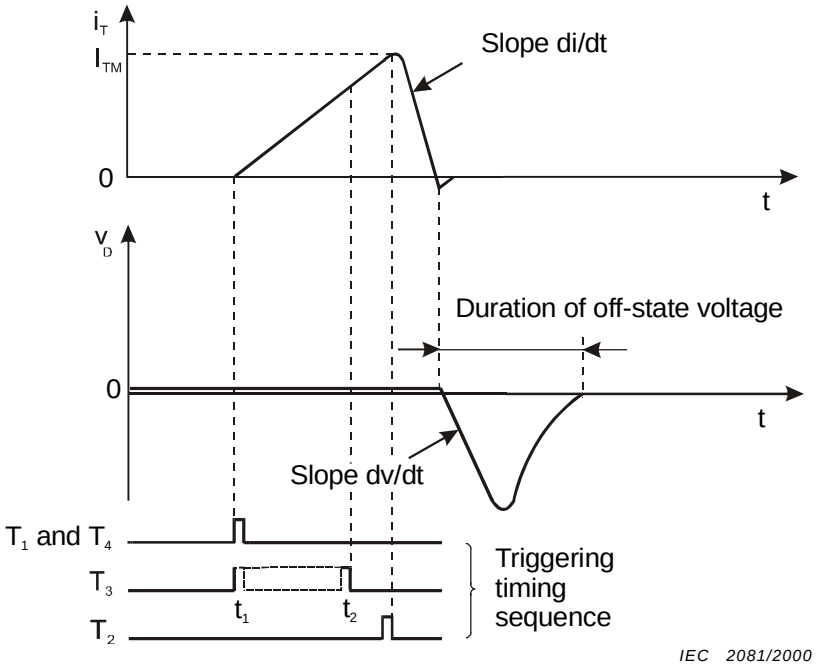
NOTE 1 High-current triacs may be defined as those rated at 50 A r.m.s. and greater.



T_4 triac being measured

NOTE 2 Other on-state current sources may be used. For example, the transformer providing V_{ac} may be replaced by a capacitor charged from a power supply.

Figure 50 – Circuit diagram for high current triacs



NOTE 3 t_1....t_2 is the time interval within which T_3 may be triggered. T_3 may not be triggered before the on-state current through T_2 has ceased, but must be triggered early enough to allow C_2 to be completely recharged, and the charging current through T_3 to have ceased before T_2 is triggered again.

Figure 51a – Waveforms with high di/dt

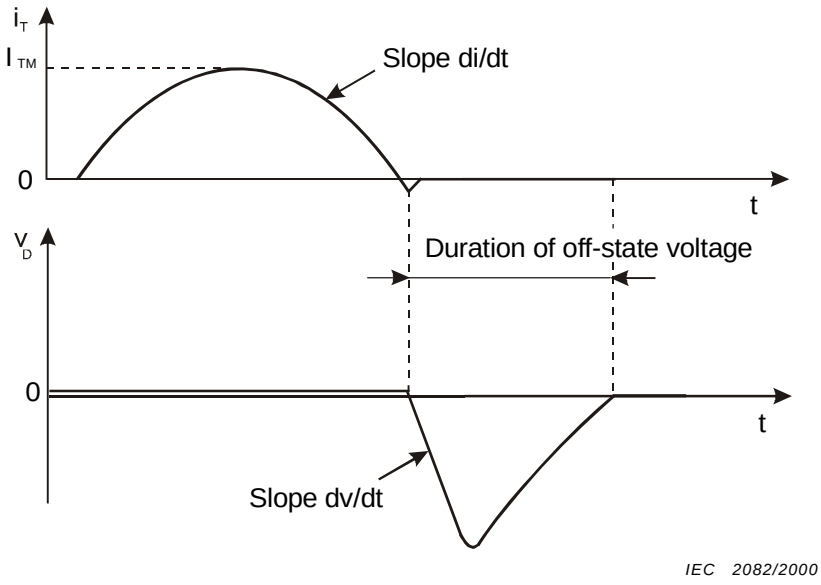


Figure 51b – Waveforms with low di/dt

Figure 51 – Waveforms with high and low di/dt

Circuit description and requirements

The on-state current I_T is supplied from the alternating supply V_{ac} via thyristor T_1, resistor R_1 and inductor L_1 to the triac T_4 being measured.

Inductor L_1 is chosen so as not to exceed the limiting value di/dt.

T_1 is triggered at the same time as the triac T_4. The off-state voltage V_D is supplied from the voltage developed across the capacitor C_2 due to the triggering of thyristor T_3 and is applied to the triac T_4 via inductor L_2 when thyristor T_2 is triggered.

The on-state current, measured across R_M by the oscilloscope, is set by adjusting V_{ac}. If T_2 is triggered during the on-state half sine wave (figure 51a) di/dt and the duration of the off-state voltage are dependent on the values of L_2 and C_2; dv/dt is dependent on the values of C_1, R_2 and E_2. If T_2 is triggered at the end of the on-state half sine wave (figure 51b) di/dt is dependent on V_{ac} and the half wave duration.

When a linear rate of rise of commutating voltage is specified, refer to 9.1.10.1 method 1 for specification of required linearity. In this case, source E_1 clamps the off-state voltage V_D.

When an exponential rate of rise of commutating voltage is specified, refer to 9.1.10.1 method 2, for permitted waveshapes. In this case, E_1 and D_1 shall be omitted and the value of V_D is obtained from the setting of E_2.

Precautions to be observed

Care must be taken to ensure that stray capacitance to earth, due to heatsinks, etc., does not affect the measurements.

The repetition frequency shall be low enough to prevent significant rise of junction temperature of the triac being measured.

The durations of the off-state voltage and the on-state current shall be long enough so that doubling them will not cause any change in the critical rate of rise of commutating voltage of the triac being measured.

Provisions, such as adding resistance in series with inductor L_2, shall be made to ensure that the triac being measured will not be destroyed if the triac cannot withstand the applied dv/dt and that capacitor C_2 discharges through the triac being measured.

Measurement procedure

All supplies are set to zero and C_1 is set to a maximum before the triac is connected into the circuit.

The temperature is set to the specified value.

Gate bias conditions are set as specified.

The on-state current is set to the specified value by adjustment of V_{ac} (for waveforms, see examples in figures 51a and 51b).

The peak off-state voltage is set to the specified value:

a) for the exponential rate of rise of voltage, by means of E_2,

b) for the linear rate of rise of voltage, clamped by means of E_1, with the value of E_2 set high enough to achieve the required linearity.

For high di/dt ($\geq$50 A/µs), T_2 is triggered during the on-state half sine wave through T_4 (figure 51a); di/dt is set to the specified value by means of L_2.

For low di/dt T_2 is triggered at an instant so that it begins to conduct on-state current at the end of the on-state half sine wave through T_4 (figure 51b).

The voltage waveform across the triac is observed on the oscilloscope (see for example figures 51a and 51b) and the rate of rise of commutating voltage is increased by adjustment of C_1 to the highest value at which the off-state voltage can be maintained across the triac without its breaking over into on state. This is the critical rate of rise of commutating voltage.

The measurement is repeated with the triac polarity reversed.

Specified conditions

a) ambient, case or reference point temperature;

b) peak on-state current (I_{TM});

c) peak off-state voltage (V_{DM});

d) gate bias conditions (during rise of commutating voltage);

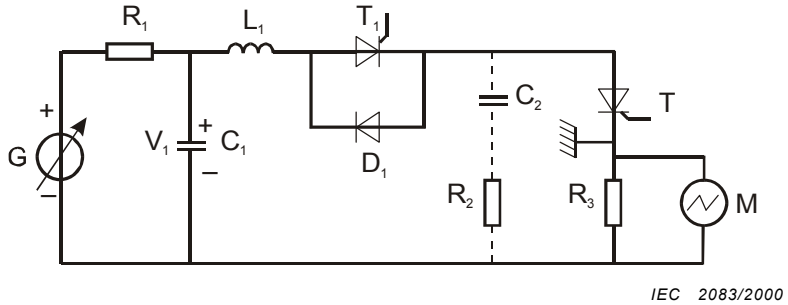
e) rate of decay of on-state current (di/dt).

9.1.13 Recovered charge (Q_r) and reverse recovery time (t_{rr})

9.1.13.1 Half sine wave method

Purpose

To measure the recovered charge Q_r and the reverse recovery time t_{rr} of a thyristor under specified conditions.



T thyristor being measured

Figure 52 – Circuit diagram for recovered charge and reverse recovery time (half sine wave method)

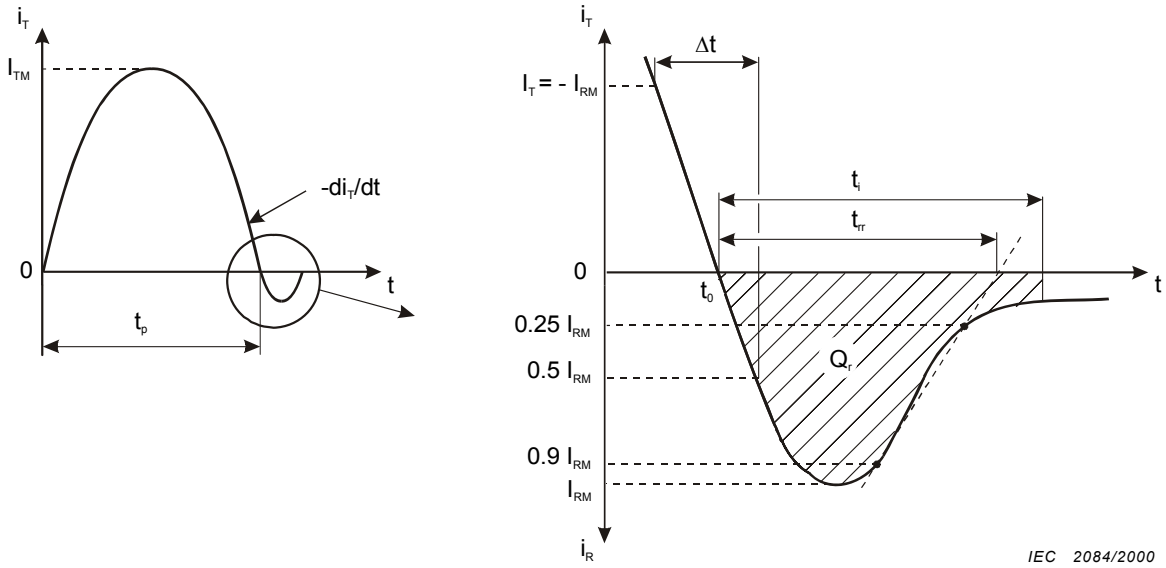


Figure 53 – Current waveform through the thyristor T

Circuit description and requirements

C_1 capacitor supplying the on-state current (see also L_1)

C_2 capacitor limiting the high induced reverse voltage

D_1 antiparallel diode

G on-state current generator

L_1 inductor adjusting the rate of change of forward current $-di_T/dt$ and the pulse duration $\left(t_p = \pi\sqrt{L_1 C_1}\right)$

M measuring instrument (for example: an oscilloscope)

R_1 resistor limiting the charge of C_1

R_2 resistor limiting the high induced reverse voltage

R_3 calibrated non-inductive current sensing resistor

T_1 electronic switch (for example: a thyristor)

Measurement procedure

Thyristor T_1 and the thyristor being measured T are simultaneously triggered; the on-state current generator G is adjusted to give the specified value of the peak on-state current I_{TM} through the thyristor T. The pulse duration t_p, the rate of change of forward current $-di_T/dt$, the voltage V_1 at the C_1 terminals shall be in accordance with the specified conditions.

The recovered charge is measured as

$$Q_r = \int_{t_0}^{t_0 + t_i} i_R \cdot dt$$

where

t_0 is the instant when the current passes through zero;

t_i is the specified integration time, preferably equal to the specified maximum value of t_{rr}.

The reverse recovery time t_{rr} is measured as the time interval between t_0 and the instant when, for decreasing values of i_R, a line through the points for 0,9 I_{RM} and 0,25 I_{RM} crosses the zero current axis.

Specified conditions

a) ambient or case temperature;
b) peak on-state current I_{TM};
c) voltage V_1 at the C_1 terminals;
d) pulse duration of on-state current t_p;
e) rate of change of on-state current $-di_T/dt$ (see note);
f) integration time t_i.
g) C_1, C_2, R_2.

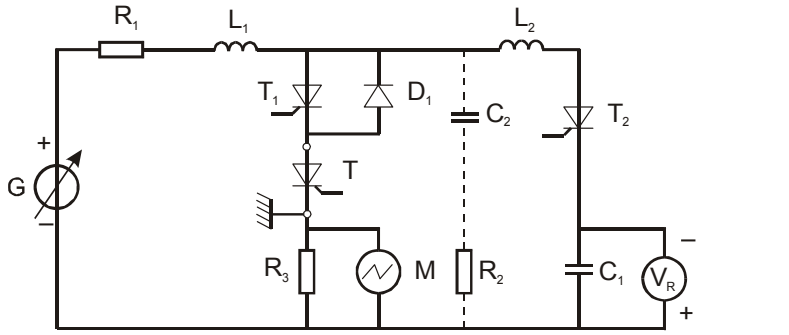
NOTE The rate of change of on-state current is measured at zero crossing current, if possible for current values between $i_T = -I_{RM}$ and $i_r = 0{,}5\ I_{RM}$. In the latter case

$$-\frac{di_T}{dt} = \frac{3}{2} \cdot \frac{I_{RM}}{\Delta t} \quad \text{(see figure 53)}$$

9.1.13.2 Rectangular wave method

Purpose

To measure the recovered charge Q_r and the reverse recovery time t_{rr} of a thyristor under specified conditions.



T thyristor being measured

Figure 54 – Circuit diagram for recovered charge and reverse recover time (rectangular wave method

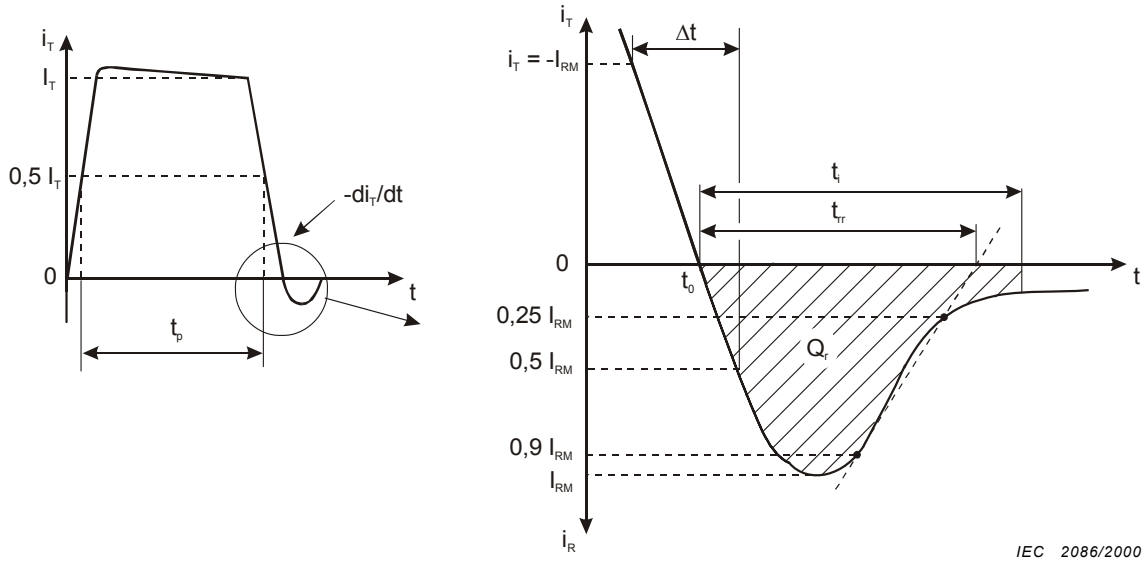


Figure 55 – Current waveform through the thyristor T

Circuit description and requirements

C_1 capacitor supplying the reverse recovery current of T

C_2 capacitor limiting the high induced reverse voltage

D_1 antiparallel diode

G on-state current generator

L_1 inductor blocking the reverse voltage (the value of L_1/R_1 is selected to be much smaller than the time t_p)

L_2 inductor adjusting the rate of change of forward current $-di_T/dt$

M measuring instrument (for example, an oscilloscope)

R_1 resistor limiting on-state current

R_2 resistor limiting the high induced reverse voltage

R_3 calibrated non-inductive current sensing resistor

T_1 and T_2 electronic switches (for example, thyristors)

Measurement procedure

Thyristor T_1 and thyristor being measured T are simultaneously triggered and the on-state current generator G is adjusted to give the specified value of on-state current I_T before triggering T_2.

Thyristor T_2 is triggered after the time t_p and the current through the thyristor T is reversed by means of an externally applied reverse voltage V_R.

The rate of change of forward current is adjusted to the specified value by means of the reverse voltage V_R in association with capacitor C_1 and inductor L_2.

The recovered charge is measured as

$$Q_r = \int_{t_0}^{t_0+t_i} i_R \cdot dt$$

where

t_0 is the instant when the current passes through zero;

t_i is the specified integration time, preferably equal to or greater than the specified maximum value of t_{rr}.

The reverse recovery time t_{rr} is measured as the time interval between t_0 and the instant when, for decreasing values of i_R, a line through the points for 0,9 I_{RM} or, if specified, I_{RM} and 0,25 I_{RM} crosses the zero current axis.

Specified conditions

a) ambient or case temperature;
b) on-state current (before triggering T_2) I_T;
c) reverse voltage V_R;
d) pulse duration of on-state current t_p;
e) rate of change of on-state current $-di_T/dt$ (see note);
f) integration time t_i;
g) L_1, L_2, C_2, R_2.

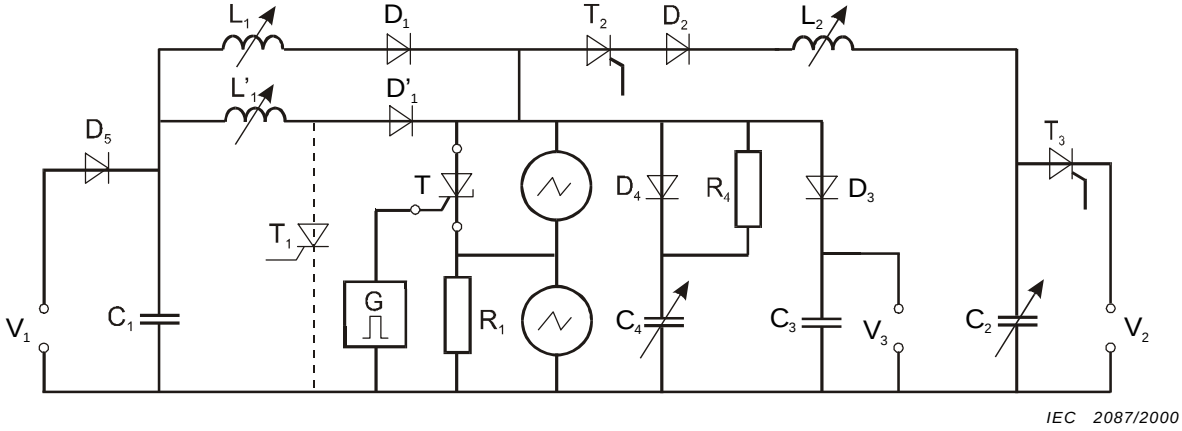
NOTE The rate of change of on-state current is measured at zero crossing current, if possible for current values between $i_T = -I_{RM}$ and $i_R = 0{,}5\ I_{RM}$. In the latter case

$$-\frac{di_T}{dt} = \frac{3}{2} \cdot \frac{I_{RM}}{\Delta t} \quad \text{(see figure 55)}$$

9.1.14 Circuit commutated turn-off time (t_q) of a reverse conducting thyristor

Purpose

To measure the circuit commutated turn-off time of a reverse conducting thyristor (where a diode is integrated with a thyristor on a common silicon chip) or of an (asymmetrical) reverse blocking thyristor with an inverse diode connected under specified conditions.



T reverse-conducting thyristor or thyristor with inverse diode being measured

Figure 56 – Circuit diagram for measuring circuit commutated turn-off time of reverse conducting thyristor

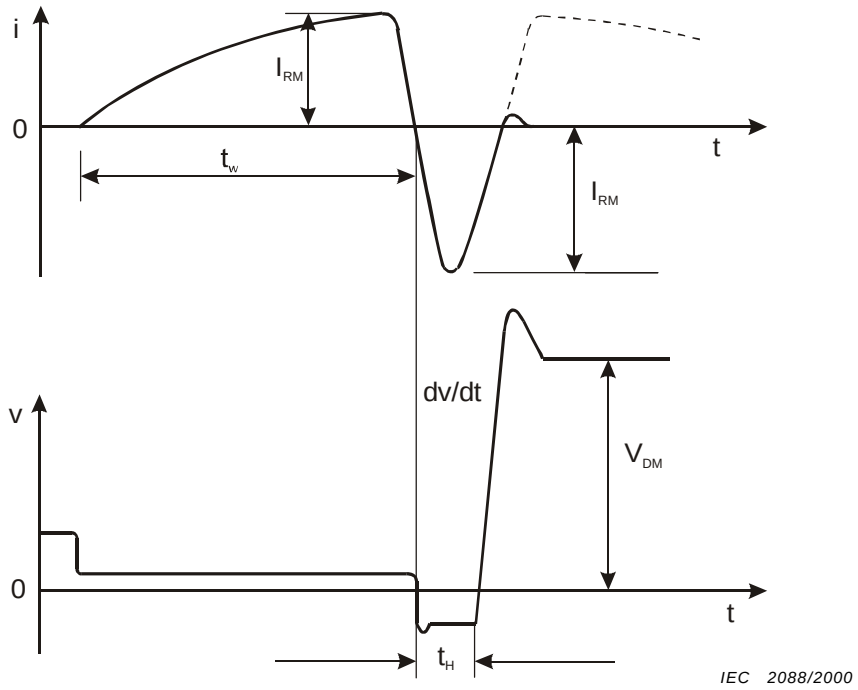


Figure 57 – Current and voltage waveforms of commutated turn-off time of reverse conducting thyristor

Circuit description and requirements

V_1	on-state current source
V_2	reverse current source
V_3	voltage for clamping the reapplied off-state voltage
C_1, L_1, L'_1	oscillating circuit to produce the on-state current half wave
C_2, L_2	oscillating circuit to produce the reverse current half wave
C_4	capacitor determining the rate of rise of the reapplied off-state voltage
T_1	thyristor to reduce the current through the thyristor being measured when it breaks over
T_2	thyristor to initiate reverse conduction
G	trigger pulse generator
R_1	non-inductive current sensing resistor
T	thyristor being measured
D_1,D'_1,	
D_2, D_3, D_4	fast recovery diodes

The capacitors C_1 and C_2 are charged during the same half cycle of the voltages V_1 and V_2 (T_3 shall be triggered). During the following half cycle, the thyristor being measured is triggered and conducts a quarter sine wave, the form of which is determined by V_1, C_1 and L_1 (and L'_1).

At the instant when the on-state current reaches its crest value I_{TM}, thyristor T_2 is triggered. The current through the thyristor being measured reverses. The half sine wave reverse current is determined by V_2, C_2 and L_2. Its duration determines the hold-off interval t_H (see figure 57).

After the reverse current half wave, the current from C_1 and L_1 charges capacitor C_4 almost linearly. The rate of rise of the voltage across C_4 is determined by the charging current and by the value of C_4, and may be varied by adjusting C_4. The peak value V_{DM} is limited by the clamping voltage V_3. Diode D_1 prevents C_4 from discharging so that the voltage across the thyristor being measured remains at V_{DM} for some time.

The value of R_4 shall be high enough to limit the discharge current from C_4 when the thyristor being measured breaks over.

It is advisable to divide L_1, D_1 and L'_1, D'_1 and to add the auxiliary thyristor T_1 which is triggered together with T_2, so that when the forward voltage is reapplied, only a small part of the current from C_1 charges C_4 (which may be made rather small in this case) or flows through the thyristor being measured when it breaks over.

Measurement procedure

– the temperature is set to the specified value,

– the trigger pulse generator is switched on,

– the on-state current through the thyristor being measured is set to the specified value by adjusting V_1 and L_1,

– the reverse current is set to the specified value by adjusting V_2, L_2 and C_2,

– the peak value of the reapplied off-state voltage is set to the specified value by adjusting V_3,

– the rate of rise of off-state voltage is set to the specified value by adjusting C_4,

– by adjusting L_2 and C_2, the hold-off interval t_H is reduced so that the device just does not break over. The value of t_H is the circuit commutated turn-off time t_q.

NOTE The voltage V_2 must be higher than V_{DM} to make sure that the current from C_1 does not flow into C_2 after commutation.

Specified conditions

The values of the following conditions should be specified:

a) case or reference point temperature;
b) peak on-state current I_{TM};
c) duration t_w of the on-state current (quarter sine wave);
d) peak reverse current I_{RM};
e) reapplied off-state voltage V_{DM};
f) rate of rise of the reapplied off-state voltage dv/dt;
g) gate circuit conditions.

9.1.15 Turn-off behaviour of GTO thyristors

Purpose

To measure the (gate-controlled) turn-off delay time (t_{dq}), the (gate-controlled) turn-off time (t_{gq}), the tail time (t_z), the (gate-controlled) fall time (t_{fq}) and the tail current (I_{ZM}) of a gate turn-off thyristor under specified conditions.

Circuit diagram and current and voltage waveforms

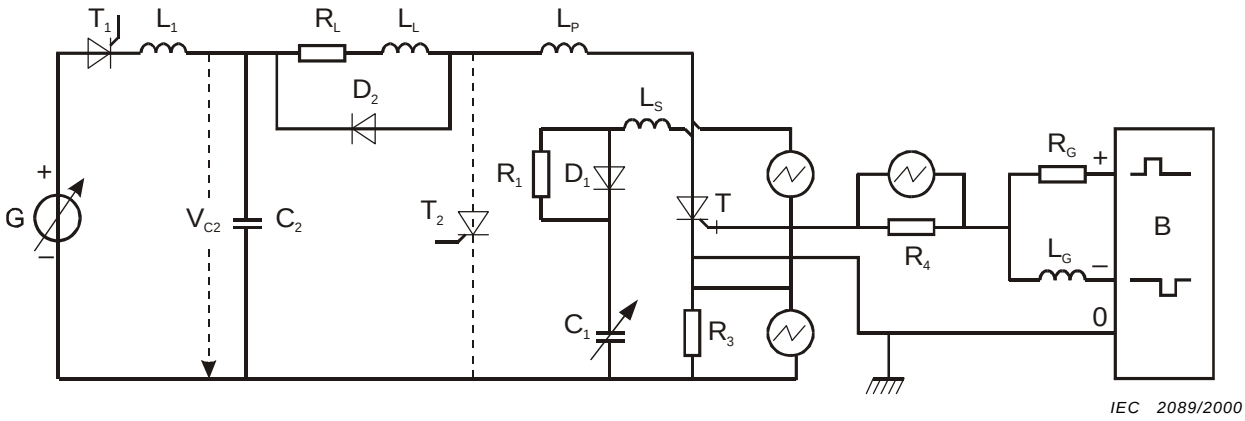


Figure 58 – Circuit diagram to measure turn-off behaviour of GTO thyristors

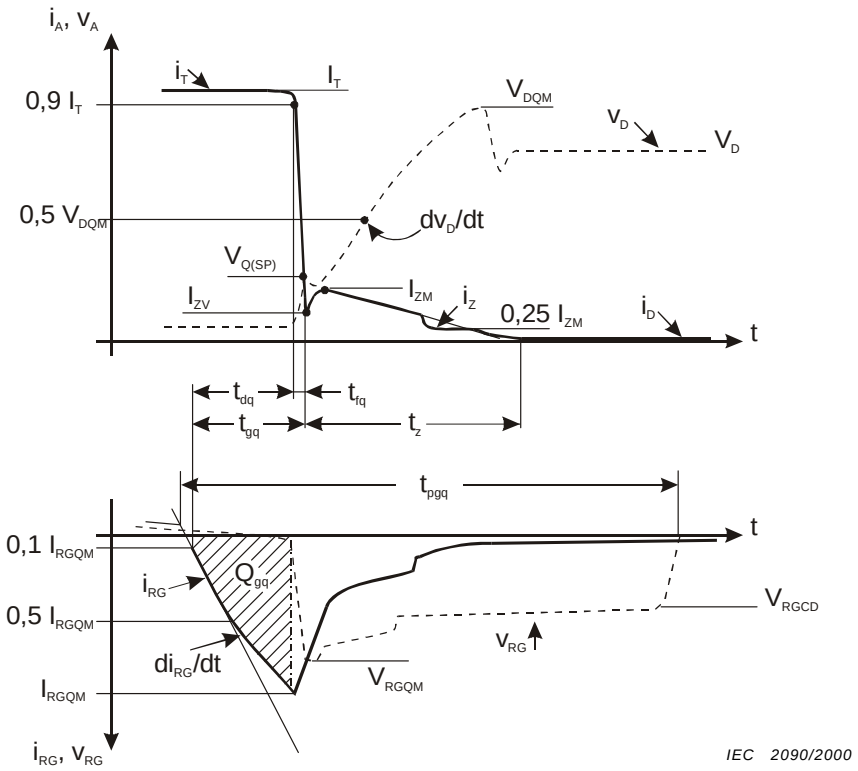


Figure 59 – Voltage and current waveforms during turn-off

Circuit description and requirements

G d.c. current supply with low internal resistance

C_2 charging capacitor with high capacitance and voltage V_{C2}

R_L, L_L load resistance and inductance which define the rate of rise di/dt and the peak value I_{TM} of the on-state current:

$$di/dt = \frac{V_{C2}}{L_L + L_P}$$

$$I_{TM} = \frac{V_{C2}}{R_L}$$

C_1 snubber capacitor used to adjust the rate of rise of the re-applied off-state voltage dv_D/dt during turn-off:

$$dv_D/dt = \frac{I_{TM}}{C_1}$$

R_1 snubber resistor to limit rate of discharge of C_1 during turn-off

D_1 snubber diode to bypass the snubber resistor during turn-off

T_1 auxiliary thyristor to charge C_2

L_1 inductance to limit di/dt through T_1

D_2 free wheeling diode

T_2 protective thyristor

R_3 measuring shunt for the principal current

R_4 measuring shunt for the gate current

B trigger circuit for turn-on and turn-off

R_G total resistance between gate and voltage source of the trigger circuit (including connections)

L_G inductance to keep the turn-off gate current I_{RGQ} constant when the internal resistance of the thyristor rises during turn-off

L_S inductance of the snubber network

L_P parasitic inductance (see under "*precautions*")

By triggering T_1, the capacitor C_2 is charged from the direct current supply G. With T_1 turned off, the GTO under test T is triggered by the forward gate current I_{FG} to conduct the specified on-state current I_{TM}.

This on-state current is turned off at the end of the chosen conduction time by the turn-off gate current I_{RGQ}.

As a consequence the voltage across the device under test T rises with the set dv_D/dt to V_{DQM}. This measurement procedure can be performed periodically as well as non-recurrently.

NOTE The current conduction time should be such that when increasing it by a factor of 2, no change in the measured turn-off time interval nor in the tail current will occur.

Precautions

The parasitic inductance L_P between the device under test T and the free wheeling diode D_2 should be minimized so that the difference between the voltage V_{DQM} across T and the voltage V_{C2} across C_2 is as small as possible.

When measuring periodically, the repetition frequency should be chosen such that no increase in the junction temperature of the GTO is observed.

The circuit set-up shall be made carefully so as to avoid overloading the device under test. This is especially important with respect to the protection circuit branch C_1, D_1, whose parasitic inductance and diode voltage determine the value of the turn-off spike voltage. Care should be taken not to exceed a safe value as defined by the manufacturer.

Precautions should be taken to prevent the device under test from being destroyed due to retriggering when it does not withstand the blocking voltage during turn off. To ensure this, a protective thyristor T_2 can be used.

Measurement procedure

The case temperature is fixed at the specified value.

The trigger circuit for the thyristor T_1 and gate drive circuit for the GTO T are synchronized so that the repetition frequency f_0 results.

The current source G is set to deliver a specified load current. By adjusting the load circuit (R_L and L_L) components respectively, the necessary off-state voltage V_{DQM} is achieved.

The rate of rise of the off-state voltage is fixed at the specified value by varying C_1.

Then the turn-off spike voltage $V_{Q(SP)}$ is checked.

L_S is adjusted to the specified value.

V_{C2} is adjusted to obtain the specified V_D value.

L_P is adjusted to obtain the specified V_{DM} value.

The turn-off delay time, the tail time, the fall time and the tail current can be viewed with a dual trace oscilloscope.

In addition the peak turn-off gate current can be viewed with an additional oscilloscope.

Turn-off conditions which retrigger the device under test during reapplication of the off-state voltage should be avoided. This should only be done when evaluating limiting values.

Specified conditions

a) case temperature (T_c);
b) repetition frequency f_0;
c) duration and amplitude I_{TM} of the on-state current;
d) peak value V_{DQM} of the off-state voltage;
e) conditions of the trigger circuit B;
f) rate of rise di_{GQ}/dt of the turn-off gate current;
g) rate of rise dv_D/dt of the off-state voltage or alternatively value of the snubber capacitor C_1;
h) parasitic inductance L_S of the snubber network in combination with the turn-off spike voltage $V_{Q(SP)}$.

9.1.16 Total energy loss during one cycle (for fast switching thyristors)

The methods for verifying the maximum rated on-state current at high switching frequencies as described in 9.3.4 can also be used to determine the total energy loss E_p during one cycle of the switching frequency. This energy loss is

$$E_p = \int_0^{t_w} v(t) \cdot i(t) \cdot dt$$

where

v(t) is the voltage across the thyristor;

i(t) is the current flowing through the thyristor;

t_w is the duration of one cycle.

In practice, it is difficult to determine E_p from the above equation, and so the following procedure may be used instead.

A direct on-state current is passed though the thyristor such that the same temperature is reached at the reference point on the case as was measured previously with the thyristor under pulse operation. Both temperature measurements shall be made under exactly the same cooling conditions and under the same thermal equilibrium conditions.

The product of the direct on-state current and the on-state voltage of the thyristor under test is the same as the total power dissipation in the thyristor under pulse operation.

The total energy loss during one cycle is calculated by dividing the total power dissipation by the repetition frequency.

9.2 Measuring methods for thermal characteristics

NOTE 1 Where applicable (methods A, B, and C), the descriptions apply to both case-rated and ambient-rated thyristors. For this, they are written in terms of the "reference point temperature T_r", where T_r may be either T_c or T_a.

NOTE 2 For easier legibility, the subscript "vj" for "virtual junction" has been shortened to "j".

9.2.1 Measurement of the case temperature

If the reference point is a hole that has been drilled by the manufacturer for this purpose, the case temperature is measured by means of a thermo-sensor (e.g. a thermocouple) inserted into this hole.

The thermocouple bead should be formed by welding rather than by soldering or twisting. The bead is inserted into the hole which is then closed over the thermocouple bead by tapping the metal at the edges of the hole (peened closed).

For other devices, the temperature at the reference point is measured by means of a temperature-sensitive element having negligible thermal capacitance, which is cemented, soldered, clamped or held rigidly against the reference point so as to ensure a negligible thermal resistance.

9.2.2 Measuring methods for thermal resistance (R_{th}) and transient thermal impedance (Z_{th})

A Methods using a temperature-sensitive characteristic of the thyristor as an indicator of the virtual junction temperature

Method A

As a temperature-sensitive characteristic, the on-state voltage of the thyristor at a small percentage of rated on-state current is used. The available sensitivity is about –2 mV/ °C.

This method is less suitable for thyristors with large wafer diameters for the following reason: during the measuring period at the low reference current, the active area is reduced to an unknown and much smaller size which varies with temperature and time.

Method B

The method also uses the on-state voltage of the thyristor as the temperature-sensitive characteristic but at a value of the reference current that is typically larger than the rated on-state current. It is well suited for thyristors with larger wafer diameters and for all GTO thyristors. The available sensitivity is about +6 mV/ °C.

Method C (for GTO thyristors only)

The method uses the avalanche voltage on the gate at a reference gate current pulse as a temperature-sensitive characteristic. It is suitable for GTO thyristors if they have, as usual, an avalanche characteristic at the gate. The available sensitivity is about +20 mV/ °C.

B Measurement by means of a heat-flow

Method D (for R_{th} only)

The method is applicable for all thyristors in disc type housings with cooling from the anode side and cathode side. The method allows the separate measurement of the thermal resistances between virtual junction and cathode side ($R_{th(j-c)K}$) and between virtual junction and anode side ($R_{th(j-c)A}$).

9.2.3 Method A

9.2.3.1 Thermal resistance (R_{th})

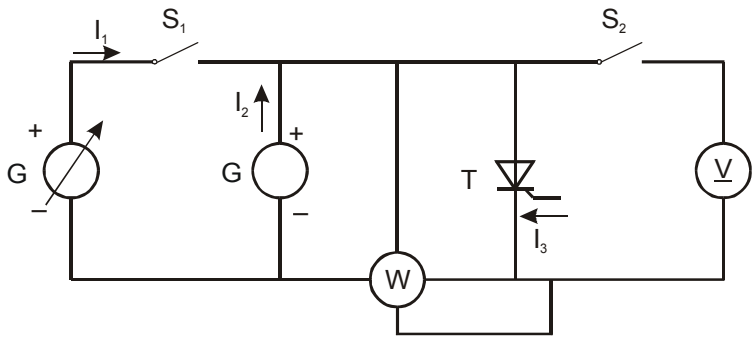
Purpose

To measure the thermal resistance of a thyristor between the virtual junction and a reference point.

Principle of the method

The temperatures $T_r(1)$ and $T_r(2)$ at the reference point are measured for two different power losses P(1) and P(2) and cooling conditions causing the same virtual junction temperature. The on-state voltage at a reference current is used to verify that the same virtual junction temperature has been reached. Then:

$$R_{th} = \frac{T_r(1) - T_r(2)}{P(2) - P(1)}$$



IEC 2091/2000

Figure 60 – Basic circuit diagram for the measurement of R_{th} (method A)

Circuit description and requirements

T thyristor being measured

I_1 heating current, either a direct or an alternating current

I_2 reference direct current monitored when the heating current is interrupted periodically for short time gaps

I_3 trigger current to maintain the thyristor in an on-state, continuous or pulsed condition (pulsed conditions to be specified)

W wattmeter to indicate the total power loss P in the junction during the heating periods (for the a.c. method, W measures the average power loss)

S_1 electronic switch to interrupt periodically the heating current I_1 (for the d.c. method); for the a.c. method, switch S_1 is not mandatory

S_2 electronic switch which is closed when the heating current I_1 is interrupted

V null – method voltmeter

Precautions to be observed

– Voltage transients occur due to excess charge carriers when the heating current is interrupted. Additional voltage transients occur if the case of the device under test contains ferromagnetic material. The switch S_2 shall not be closed before these transients have disappeared.

– Generally, the reference current I_2 shall be sufficiently high to hold the whole junction area in the on-state. To check this, it is necessary to ensure that the current remains stable immediately following the step changes in the terminal voltages such as when the heating current is interrupted and the on-state voltage of the thyristor being measured falls rapidly from a relatively higher value to a lower value.

Measurement procedure

The device to be measured is mounted in such a way that the reference point temperature can be sufficiently stabilized at a fixed value, and measured as required in 9.2.1.

The measurement is carried out in two steps:

The reference point is maintained at an elevated temperature $T_r(1)$. A low heating current is applied causing the total power loss P(1) in the junction. After reaching thermal equilibrium, the null-method voltmeter V is adjusted for zero balance. $T_r(1)$ and P (1) are recorded.

The reference point is maintained at a lower temperature $T_r(2)$. The heating current is raised until the total power P(2) warms up the junction to the same temperature as during step 1. This is indicated by zero balance of the null-method voltmeter V. $T_r(2)$ and P (2) are recorded.

The thermal resistance is calculated using the expression:

$$R_{th} = \frac{T_r(1) - T_r(2)}{P(2) - P(1)}$$

9.2.3.2 Transient thermal impedance (Z_{th})

Purpose

To measure the transient thermal impedance of a thyristor between the virtual junction and a reference point.

Principle of the method

A calibration curve is established that shows for thermal equilibrium the on-state voltage at a reference current I_2 as a function of the reference-point temperature.

The transient thermal impedance $Z_{th}(t)$ is calculated by means of the calibration curve from the values of on-state voltage and reference-point temperature at the beginning and the end of a cooling time t that follows a heating period in which the thyristor was heated by a measured power to reach thermal equilibrium.

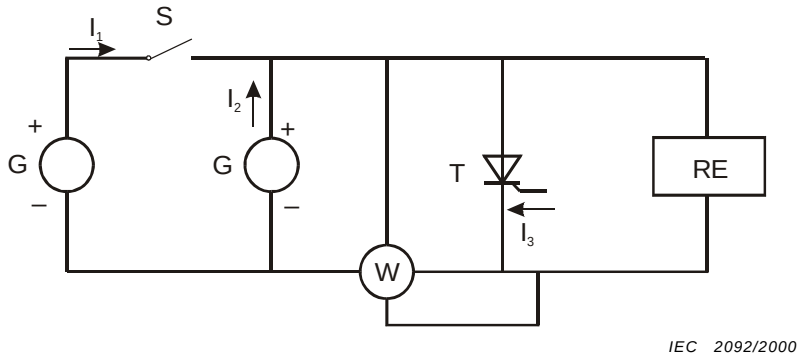


Figure 61 – Basic circuit diagram for the measurement of $Z_{th}(t)$ (method A)

Circuit description and requirements

T thyristor being measured

I_1 heating current

I_2 reference direct current

I_3 trigger current

S electronic switch to interrupt the heating current I_1

W wattmeter to indicate the total power loss in the junction during the heating period

RE recording equipment, for example an oscilloscope to record the time variation of the forward voltage V_T caused by I_2

Precautions to be observed

Generally the reference current I_2 shall be sufficiently high to hold the whole junction area in the on state.

Measurement procedure

The thyristor to be measured is mounted in such a way that the reference point temperature can sufficiently be stabilized at a fixed value and can be measured in accordance with the requirements stated in 9.2.1.

With switch S opened, I_2 is adjusted to the fixed value. The calibration curve (see the note below)

$$V_T^* = f(T_r^*)$$

is established by measuring the on-state voltage V_T^* generated at thermal equilibrium by the reference current I_2 as a function of the externally varied reference point temperature T_r^*.

The heating current I_1 is applied by closing switch S. After thermal equilibrium has been reached, the power loss in the thyristor P(0) and the on-state voltage $V_T(0)$ at t = 0 are recorded.

At t = 0 (start of the cooling period) the heating current is interrupted by opening switch S. The on-state voltage generated by I_2 is recorded as a function of the cooling time. The course of the reference-point temperature shall also be recorded if the latter cannot be sufficiently stabilized.

After the new thermal equilibrium is sufficiently reached, the power loss is again recorded (P(t)).

NOTE Values referring to the calibration curve are indicated by an asterisk * next to the letter symbol.

For a given cooling time t, the transient thermal impedance is calculated using the equation;:

$$Z_{th}(t) = \frac{\left[Tr^*(0) - Tr^*(t)\right] - \left[Tr(0) - Tr(t)\right]}{P(0) - P(t)}$$

where

T_r^* (0) or T_r^* (t) are taken from the calibration curve for values of V_T^* equal to the measured values of $V_T(0)$ or $V_T(t)$ respectively;

$T_r(0)$ and $T_r(t)$ are the measured values of T_r at t = 0 and t = t, respectively.

9.2.4 Method B

9.2.4.1 Principles of the measuring method

Measurement of the virtual junction temperature (T_j)

To measure the value T_{jm} at a given instant t_m, a sinusoidal half wave current pulse is superimposed on the actual on-state current flowing at this instant that meets the following requirements (see figure 62).

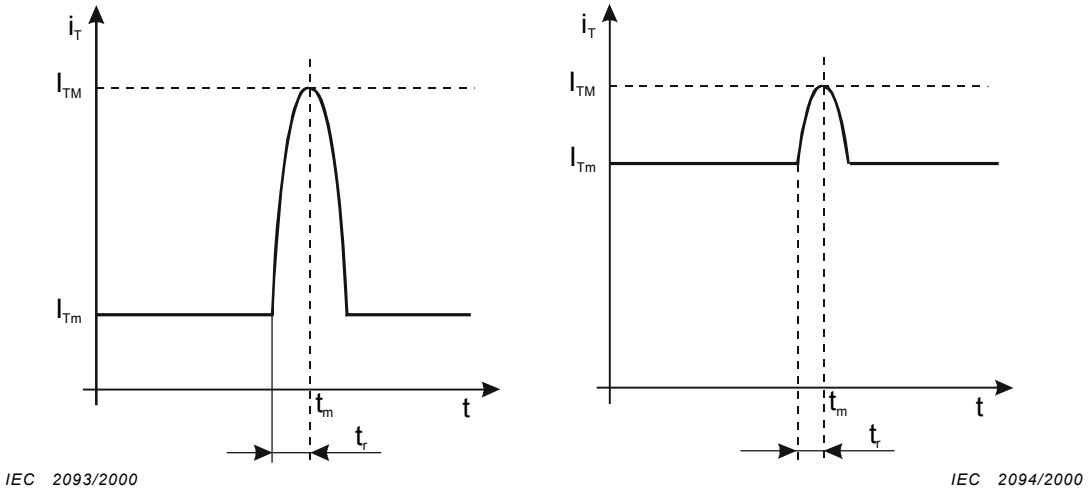


Figure 62a – With low level of I_{Tm}

Figure 62b – With high level of I_{Tm}

Figure 62 – Superposition of the reference current pulse on different on-state currents

The peak value of the current pulse I_{TM} is reached at $t = t_m$. For this, the pulse starts at $t = t_m - t_r$ where t_r is the rise time of the pulse to its peak value.

The pulse duration $2t_r$ is small compared with the thermal time constant of the silicon chip, but also sufficiently large so that after t_r equilibrium of the charge carriers in the thyristor has been reached.

The amplitude of the added pulse is controlled so that, independently of the pre-load I_{Tm}, always the same peak value I_{TM} (reference measuring current) is reached.

The value of I_{TM} shall typically be larger than the value of the rated on-state current.

The superimposed power dissipation during the current pulse leads to a superimposed rise of virtual junction temperature which possibly cannot be neglected. Figure 63 shows this for the more general case where, after P had been reduced at t = 0 from P(1) to the lower value P(2), thermal equilibrium would not yet be reached at $t = t_m$.

The solid line in figure 63b shows this additional rise ΔT_j which reaches the value ΔT_{jm} at $t = t_m$.

Figure 63c shows the course of the virtual junction temperature T_j that results from the linear addition of ΔT_j to T_j.

At $t = t_m$, the value $T'_{jm} = T_{jm} + \Delta T_{jm}$ is reached and this value is measured by means of a calibration curve. The value to be measured shall then be calculated as

$$T_{jm} = T'_{jm} - \Delta T_{jm} \quad (1)$$

For this, a sufficiently accurate value of ΔT_{jm} can be calculated from known typical parameter values of the thyristor.

Due to the linear superposition of ΔT_j on T_j, the value of T'_{jm} does not depend on whether thermal equilibrium would already have been reached at t_m or not. Thus, the measuring method is applicable to the measurement of both R_{th} and $Z_{th}(t)$.

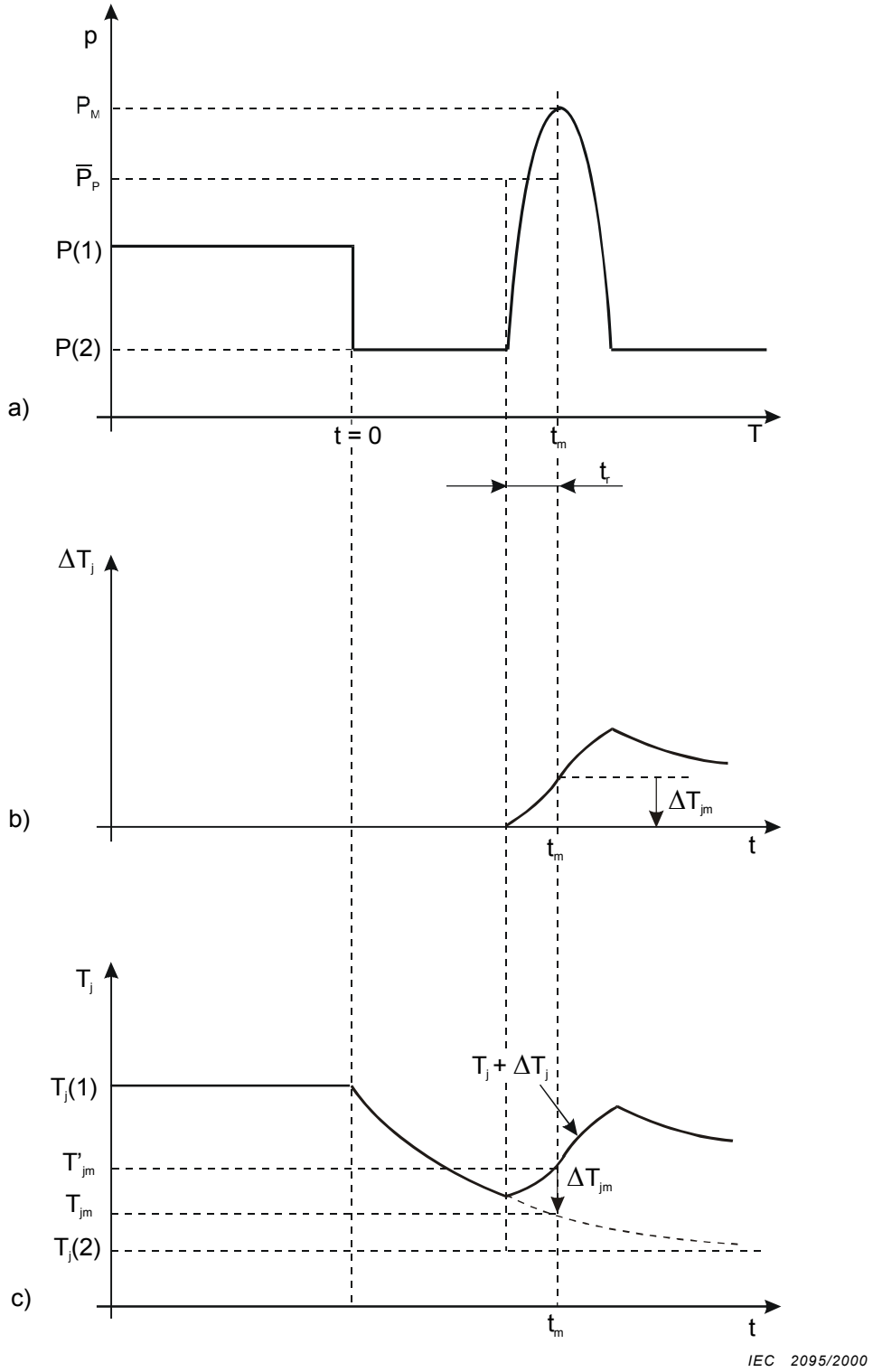


Figure 63 – Waveforms for power loss and virtual junction temperature (general case)

Calculation of ΔT_{jm}

If the requirements listed above are met, the course of P during t_r can be replaced by a constant power loss, ($\overline{P}_P$, dashed line in figure 63a) that equals the mean value of the actual power loss during t_r. In a first-order approximation it shall further be supposed that the actual course of the superimposed power loss has also the form of a sine wave.

Then
$$\overline{P}_P - P(2) = \frac{2}{\pi}\left(P_M - P(2)\right) \tag{2}$$

$$\Delta T_{jm} = \frac{2}{\pi}\left(P_M - P(2)\right) Z_{th}\left(t_r\right) \tag{3}$$

If the straight-line approximation for the on-state characteristic is known, the factor $2/\pi$ in equation (3) can more precisely be calculated. However, this additional correction of the already rather small correction ΔT_{jm} is not necessary. In this respect, figure 63 cannot be drawn to scale. It is practical to express ΔT_{jm} as a fraction of (P_M – P(2)) R_{th}, i.e. of the maximum change of temperature that would be reached for very large values of t_r:

$$\Delta T_{jm} = \varepsilon\left(P_M - P(2)\right) R_{th} \tag{4}$$

Then (1) becomes
$$T_{jm} = T'_{jm} - \varepsilon\left(P_M - P(2)\right) R_{th} \tag{5}$$

with
$$\varepsilon = \frac{2}{\pi}\frac{Z_{th}\left(t_r\right)}{R_{th}} \tag{6}$$

Obviously, it is a disadvantage of the measuring method that the individual values of R_{th} or Z_{th} are calculated from the difference of two T_{jm} values and that for the calculation of these two values (equation (5)) the individual values of R_{th} and Z_{th} should already be known. However, as said above, the correction factor ε is so small that for its calculation typical values of R_{th} and $Z_{th}(t_r)$ can be used.

Calculation of ε

When the typical value for $Z_{th}(t_r)$ is not directly specified, ε can be calculated from other given typical parameter values, for example:

a) from the volume V of the silicon chip. If the requirements listed above are met, practically the total energy lost during t_r will be stored in the thermal capacity C_{th} of the chip; therefore:

$$\Delta T_{jm} \approx \frac{2}{\pi}\left(P_M - P(2)\right)\frac{t_r}{C_{th}} \tag{7}$$

C_{th} can be calculated from a known volume of the chip V as

$$C_{th} = V \cdot c \cdot \rho \tag{8}$$

where

V is the volume (cm^3),

c is the specific heat 0,735 (Ws/kg);

ρ is the specific density 2,34 (g/cm^3) of silicon.

Then ε results from (4) and (7)

$$\varepsilon = \frac{2}{\pi} \cdot \frac{t_r}{R_{th} C_{th}} \tag{9}$$

b) from the specified analytical function for $Z_{th}(t)$ of the form:

$$Z_{th}(t) = \sum_{i=1}^{n} R_i \left(1 - \exp\left(-t/\tau_i\right)\right) \tag{10}$$

From (10), the initial slope of $Z_{th} = f(t)$ results in:

$$\left(dZ_{th}/dt\right)_{t=0} = \sum_{i=1}^{n} R_i / \tau_i \tag{11}$$

Then $$Z_{th}(t_r) = t_r \cdot \left(dZ_{th}/dt\right)_{t=0} \tag{12}$$

and $$\varepsilon = \frac{2}{\pi} \cdot \frac{t_r}{R_{th}} \sum_{i=1}^{n} R_i / \tau_i \tag{13}$$

Recording and application of the calibration curve

NOTE 1 Values referring to the calibration curve are indicated by the superscript * next to the letter symbol.

For the recording of the calibration curve, the peak value of the reference current pulse I_{TM} and the value of a constant preload P* are chosen.

The reference point temperature T_r* is varied externally by means of electric heating at the contact plates of the thyristor or by means of heating in an oil bath. For different values of T_r* the peak value of the on-state voltage (V_{TM}*) is measured under conditions of thermal equilibrium. The calibration curve is drawn as the curve $V_{TM}^* = f(T_r^*)$, see figure 64.

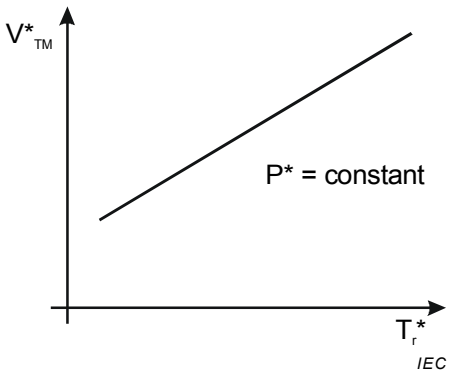


Figure 64 – Calibration curve

The measured peak value V_{TM}* corresponds very closely to the value of V_{TM} at t = t_m, so that T_{jm}* for V_{TM}* can be calculated as:

$$T_{jm}^* = T_r^* + P^* R_{th} + T_j^*$$

with equation (4) $$T_{jm}^* = T_r^* + P^* R_{th} + \varepsilon (P_M - P^*) R_{th} \quad (14)$$

For the measurement of T_{jm} at t_m, the peak value V_{TM} at t_m is measured, and for $V_{TM}^* = V'_{TM}$ the corresponding value of T_r* is taken from the calibration curve.

From $V^*_{TM} = V'_{TM}$ follows $T^*_{jm} = T'_{jm}$

Hence, with (5) and (14):

$$T_{jm} = T_r^* + P^* R_{th} + \varepsilon (P(2) - P^*) R_{th} \quad (15)$$

This equation could be used to calculate T_{jm}. However, for the present measuring method, this is not necessary because the P* terms cancel each other out when R_{th} or Z_{th} are calculated from the difference of two T_r* values.

Calculation of R_{th}

For two different power dissipations (P(1), P(2)) the reference point temperatures ($T_r(1)$, $T_r(2)$) are controlled so that in both cases at thermal equilibrium the same peak values of on-state voltage ($V_{TM}(1) = V_{TM}(2)$) and therefore the same virtual junction temperature is reached:

$$T'_{jm}(1) = T'_{jm}(2) \quad (16)$$

With (5) and

$$T_{jm} = T_r + P R_{th} \quad (17)$$

follows from (16)

$$R_{th} = \frac{1}{1-\varepsilon} \cdot \frac{T_r(1) - T_r(2)}{P(2) - P(1)} \quad (18)$$

Calculation of $Z_{th}(t)$

NOTE 2 For the calculation of $Z_{th}(t)$ the time indicators (0) and (t) are used instead of (1) or (2), respectively.

In a first measurement, with reference point temperature $T_r(0)$ and power loss P(0), $V_{TM}(0)$ is measured under conditions of thermal equilibrium.

At t = 0, the power loss is lowered abruptly to the value P(t). At the specified time t, T_r and V_{TM} are measured again ($T_r(t)$, $V_{TM}(t)$).

From the calibration curve, the values T_r*(0), T_r*(t) corresponding to $V_{TM}(0)$, $V_{TM}(t)$ are read.

Then $$Z_{th}(t) = \frac{[\ T_{jm}(0) - T_{jm}(t)\ ] - [\ T_r(0) - T_r(t)\ ]}{P(0) - P(t)} \quad (19)$$

with

$$T_{jm}(0,t) = T_r^*(0,t) + P^* R_{th} + \varepsilon (P(0,t) - P^*) R_{th} \quad (20)$$

follows from (19)

$$Z_{th}(t) = \frac{[T_r^*(0) - T_r^*(t)] - [T_r(0) - T_r(t)]}{P(0) - P(t)} + \varepsilon R_{th} \quad (21)$$

9.2.4.2 Thermal resistance (R_{th})

Purpose

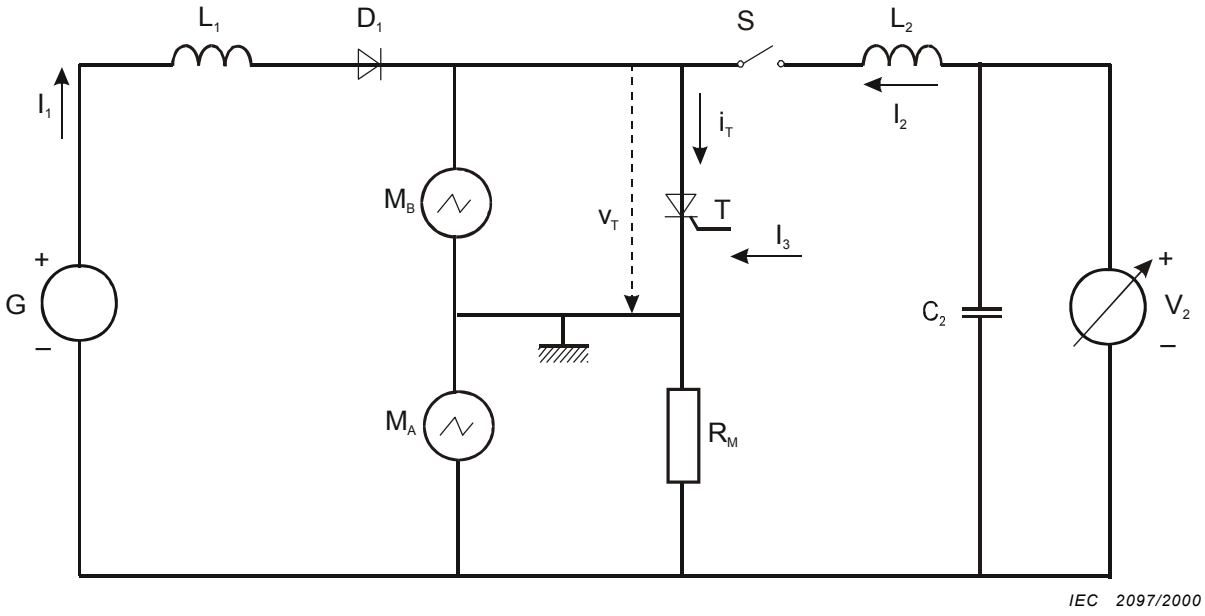
To measure the thermal resistance between the virtual junction and a reference point, preferably for high power thyristors.

Principle of the method

The temperatures $T_r(1)$ and $T_r(2)$ at the reference point are measured for two different power losses P(1) and P(2) and cooling condition causing the same junction temperature. The on-state voltage V_{TM} at the peak value of a reference current pulse is used to verify that the same virtual junction temperature has been reached.

Then: $$R_{th} = \frac{1}{1-\varepsilon} \cdot \frac{T_r(1) - T_r(2)}{P(2) - P(1)}$$

(For the significance of ε, see 9.2.4.1, equations (6) and (9))



T thyristor being measured

Figure 65 – Basic circuit diagram for the measurement of R_{th} (method B)

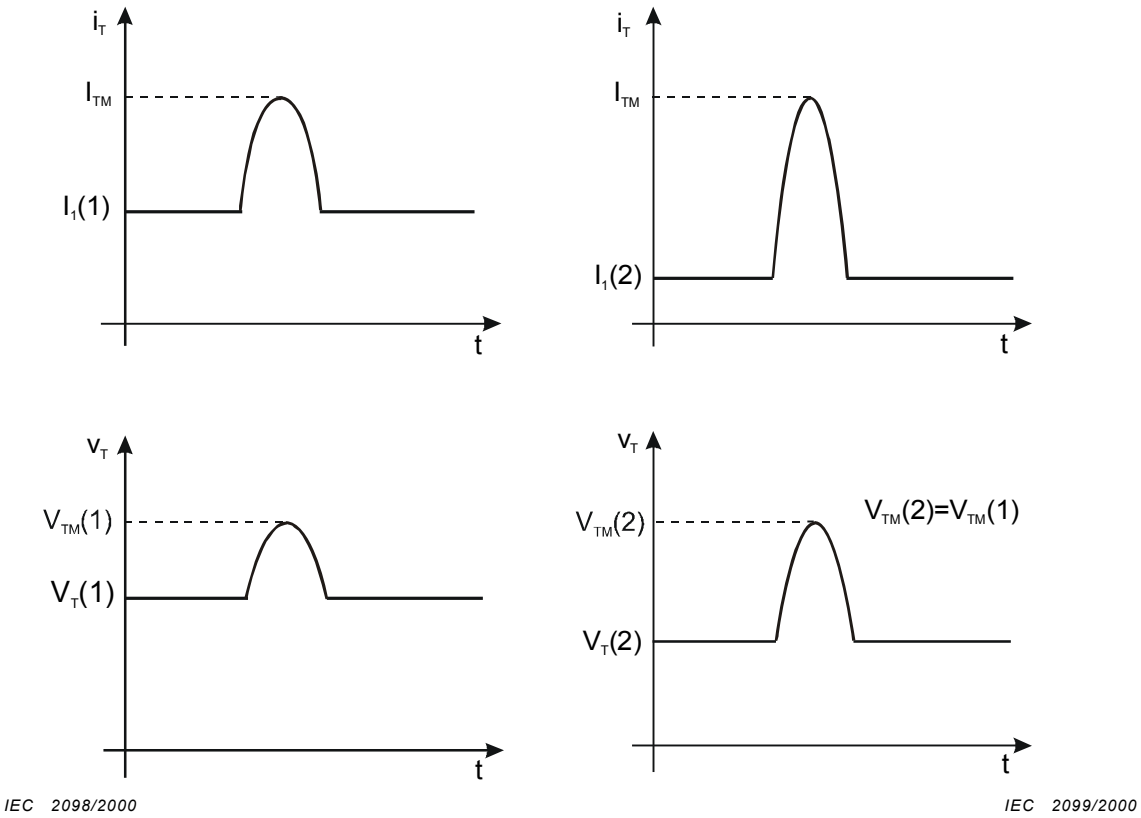


Figure 66a – Step 1

Figure 66b – Step 2

Figure 66 – Waveforms for measuring thermal resistance

Circuit description and requirements

C_2 capacitor supplying the sinusoidal reference current pulse (see also L_2)

D_1 blocking diode

G current generator for the heating current I_1 which generates the power loss P in the thyristor T

I_3 trigger current to maintain the on state

L_1 inductor, blocking the reference current pulse

L_2 inductor, determining together with C_2 the duration $2t_r$ of the reference current pulse

$$\left(2t_r = \pi\sqrt{L_2 C_2}\right)$$

M_A measuring instrument for the heating current I_1 and the reference measuring current I_{TM} (the peak value of I_T during the reference current pulse)

M_B measuring instrument for the on-state voltage V_T at the heating current I_1 and for the peak value V_{TM} produced by the reference current pulse

RM calibrated non-inductive current sensing resistor

S electronic switch

V2 voltage source for setting the peak value I_{TM} during the reference current pulse

Precautions to be observed

Generally, the duration $2t_r$ of the reference current pulse should be in the range of 1 ms to establish at its peak value equilibrium of the charge carriers in T. The interval t_r is then also sufficient for high power thyristors, since the sine wave starts from a lower current.

To obtain optimum sensitivity (mV/°C), the peak value I_{TM} of the reference current pulse shall be about three to five times the rated on-state current of the thyristor being measured.

Measurement procedure

The thyristor being measured is mounted in such a way that the reference-point temperature can sufficiently be stabilized at a fixed value, and be measured as required in 9.2.1.

The measurement is carried out in two steps (see figure 66)

Step 1: The reference point temperature is maintained at a lower value. The on-state voltage V_T is measured and the heating current is adjusted to reach the power loss $P(1) = I_1(1)\ V_T\ (1)$. The reference current pulse is adjusted so that the fixed reference measuring current (peak value I_{TM}) is reached. After thermal equilibrium has been reached, the peak value of the on-state voltage $V_{TM}(1)$ and the reference point temperature $T_r(1)$ are recorded.

Step 2: At a lower heating current $I_1(2)$ generating the power loss $P(2) = I_1(2)\ V_T(2)$ the peak value of the reference current pulse is adjusted to reach I_{TM} as before. The reference point temperature is elevated until the same peak value of the on-state voltage is reached as before: $V_{TM}(2) = V_{TM}(1)$. The reference point temperature $T_r(2)$ is recorded.

The thermal resistance is calculated using the expression

$$R_{th} = \frac{1}{1-\varepsilon} \cdot \frac{T_r\,(1) - T_r\,(2)}{P(2) - P(1)}$$

(For the significance of ε, see 9.2.4.1, equations (6) and (9). Mostly, ε can be approximated to zero.)

9.2.4.3 Transient thermal impedance ($Z_{th}(t)$)

Purpose

To measure the transient thermal impedance between the virtual junction and a reference point, preferably for high power thyristors.

Principle of the method

After applying the heating current and waiting until thermal equilibrium is established, the power loss in the thyristor, the on-state voltage at the peak value of a reference current pulse and the reference point temperature are recorded. The heating current is then lowered abruptly, and the on-state voltage at the peak value of the reference current pulse together with the reference point temperature are recorded as a function of time.

By means of a calibration curve, the recorded values of the on-state voltage are converted to corresponding values of virtual junction temperature from which the transient thermal impedance is calculated.

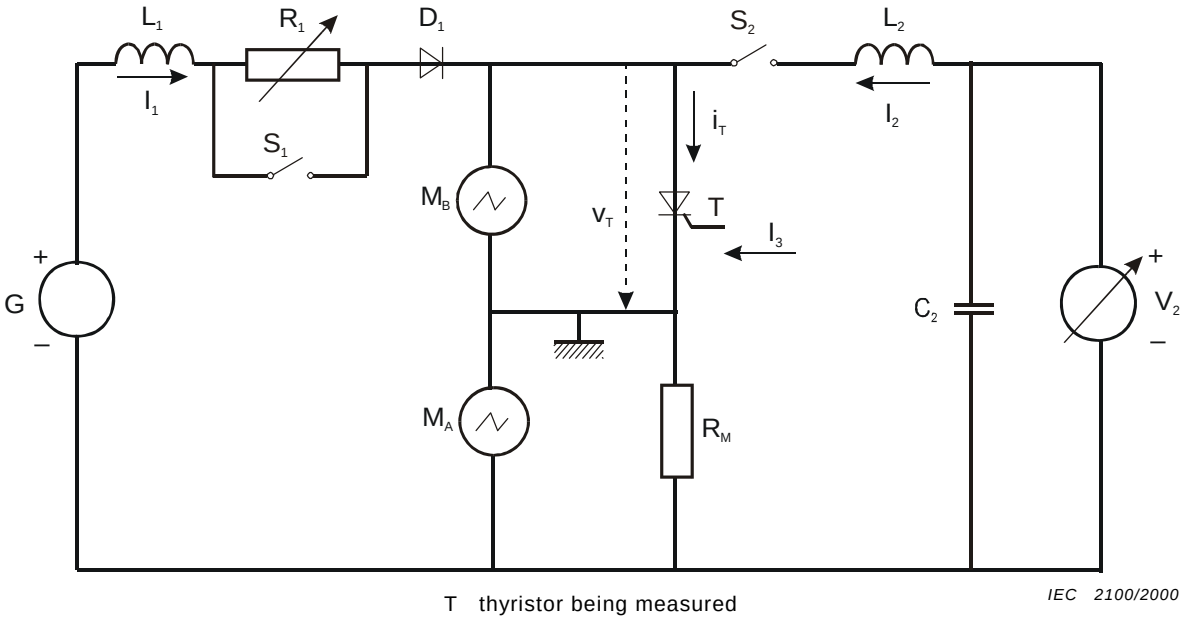


Figure 67 – Basic circuit diagram for the measurement of $Z_{th}(t)$ (method B)

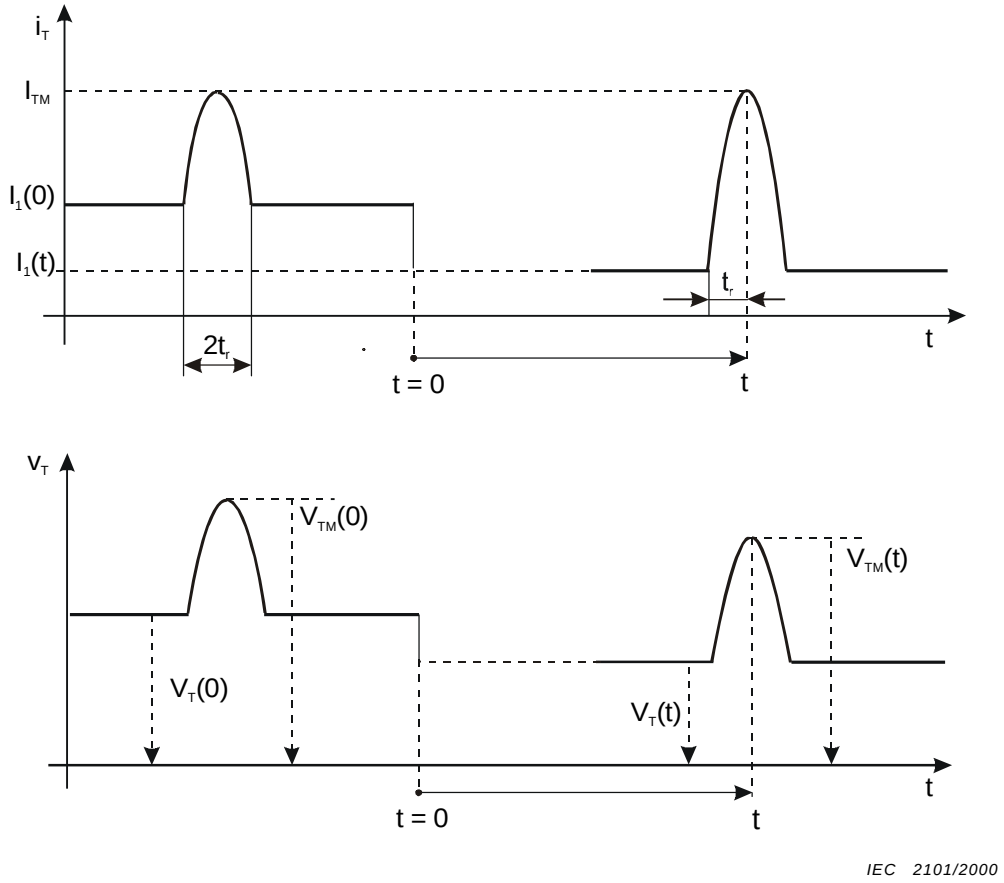


Figure 68 – Waveforms for measuring transient thermal impedance

Circuit description and requirements

C_2 capacitor supplying the sinusoidal reference current pulse (see also L_2)

D_1 blocking diode

G current generator for current I_1 during the heating period $I_1(0)$ and the cooling period $I_1(t)$

I_3 trigger current to maintain the on state

L_1 inductor blocking the reference current pulse

L_2 inductor determining together with C_2 the duration $2t_r$ of the reference current pulse

$$\left(2t_r = \pi\sqrt{L_2 C_2}\right)$$

M_A measuring instrument for the heating current I_1 and the reference measuring current I_{TM} (the peak value of I_T during the reference current pulse)

M_B measuring instrument for the on-state voltage V_T at the heating current I_1 and for the peak value V_{TM} produced by the reference current pulse

RM calibrated non-inductive current sensing resistor

R_1 resistor to adjust $I_1(t)$

S_1 electronic switch (for example a GTO)

S_2 electronic switch (for example a thyristor)

V_2 voltage source for setting the peak value I_{TM} during the reference current pulse

Precautions to be observed

Generally, the duration $2t_r$ of the reference current pulse should be in the range of 1 ms to establish at its peak value equilibrium of the charge carriers in T. The interval t_r is then also sufficient for high power thyristors, since the sine wave starts from a lower current.

To obtain optimum sensitivity (mV/°C), the peak value I_{TM} of the reference current pulse shall be about three to five times the nominal current of the thyristor being measured.

Measurement procedure

The thyristor being measured is mounted in such a way that the reference point temperature can be sufficiently stabilized and measured as required in 9.2.1.

A calibration curve is prepared as described in 9.2.4.1 above. The preload current I_T* shall have the same value as the on-state current will later have during the cooling period $I_1(t)$.

To prepare the measurement, the fixed values for current I_1 during the heating period $I_1(0)$ and the cooling period $I_1(t)$ shall be adjusted with switch S_2 opened. First, switch S_1 is closed and I_1 is adjusted to the value $I_1(0)$ by means of the variable generator G. Then switch S_1 is opened and I_1 is adjusted to the value $I_1(t)$ by means of the variable resistor R_1.

For the measurement, $I_1(0)$ is applied (switch S_1 closed). After thermal equilibrium has been reached, the actual value $I_1(0)$, the corresponding on-state voltage $V_T(0)$, the peak value $V_{TM}(0)$ and the reference point temperature $T_r(0)$ are recorded.

At the time t = 0, I_1 is lowered abruptly to the value $I_1(t)$ by opening switch S_1. At the same time, V_2 is increased so that again the fixed reference measuring current I_{TM} will be reached for the subsequent measurement of $V_{TM}(t)$. At the time t = t_r, switch S_2 is closed and at the time t the peak value $V_{TM}(t)$ at I_{TM} and $T_r(t)$ are recorded. Subsequently, the actual values of $I_1(t)$ and $V_T(t)$ are measured.

Periodic recording during the cooling period is possible if the periodical heating by the reference current pulse can be neglected.

For the calculation of $Z_{th}(t)$, the values $T_r^*(0)$ and $T_r^*(t)$ corresponding to the measured values $V_{TM}(0)$ and $V_{TM}(t)$ are taken from the calibration curve.

The transient thermal impedance is calculated (see equation (21) in 9.2.4.1) as

$$Z_{th}(t) = \frac{\left[T_r^*(0) - T_r^*(t)\right] - \left[T_r(0) - T_r(t)\right]}{P(0) - P(t)} + \varepsilon R_{th}$$

where

$P(0) = I_1(0) \cdot V_T(0)$ and

$P(t) = I_1(t) \cdot V_T(t)$.

(For the significance of ε, see 9.2.4.1, equations (6) et (9). In general, εR_{th} can be neglected.)

9.2.5 Method C (for GTO thyristors only)

9.2.5.1 Calibration curve

The calibration curve refers to the off-state characteristic of the GTO thyristor. It shows the avalanche breakdown gate voltage V_{GR}^* at a reference gate current pulse I_G^* as a function of the virtual junction temperature T_j^*. In the off state, T_j^* equals the reference point temperature T_r^*, and T_j^* is varied by varying T_r^* externally.

The peak value of the reference current pulse shall be chosen according to the size and the structure of the GTO thyristor in order to keep it in full conduction. Its duration and repetition frequency shall be chosen such that no significant temperature rise in the GTO thyristor is caused.

9.2.5.2 Thermal resistance (R_{th})

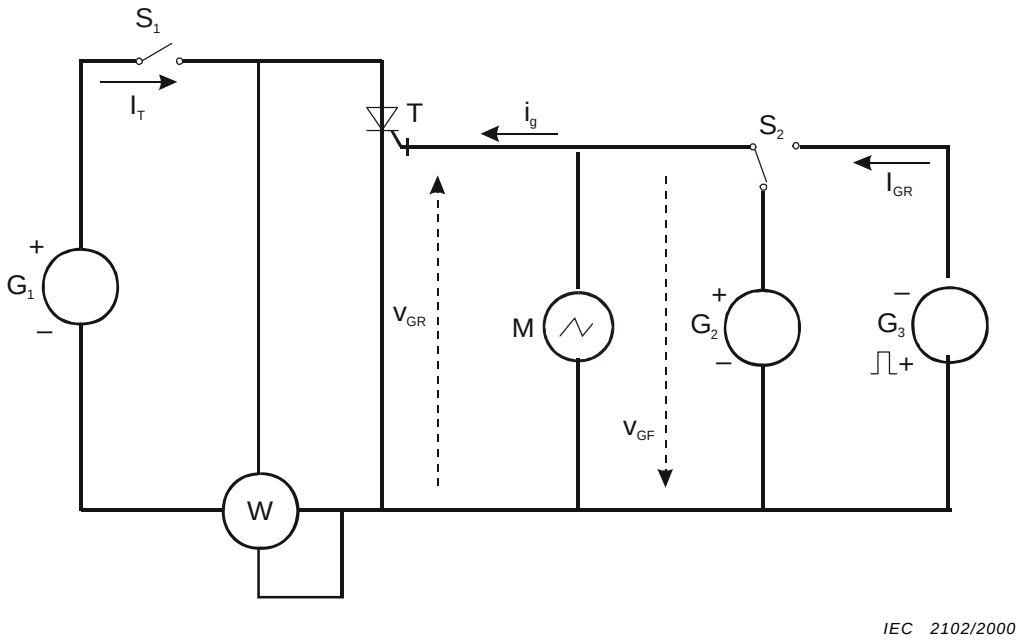
Purpose

To measure the thermal resistance of a gate turn-off thyristor between the virtual junction and a reference point.

Principle of the method

The temperatures $T_r(1)$ and $T_r(2)$ of the reference point are measured for the power loss P and zero, respectively and cooling conditions causing the same junction temperature. The avalanche voltage on the gate at a reference current pulse is used to verify that the same junction temperature has been reached.

Then $$R_{th} = \frac{T_r(2) - T_r(1)}{P}$$



T thyristor being measured

Figure 69 – Basic circuit diagram for the measurement of R_{th} (method C)

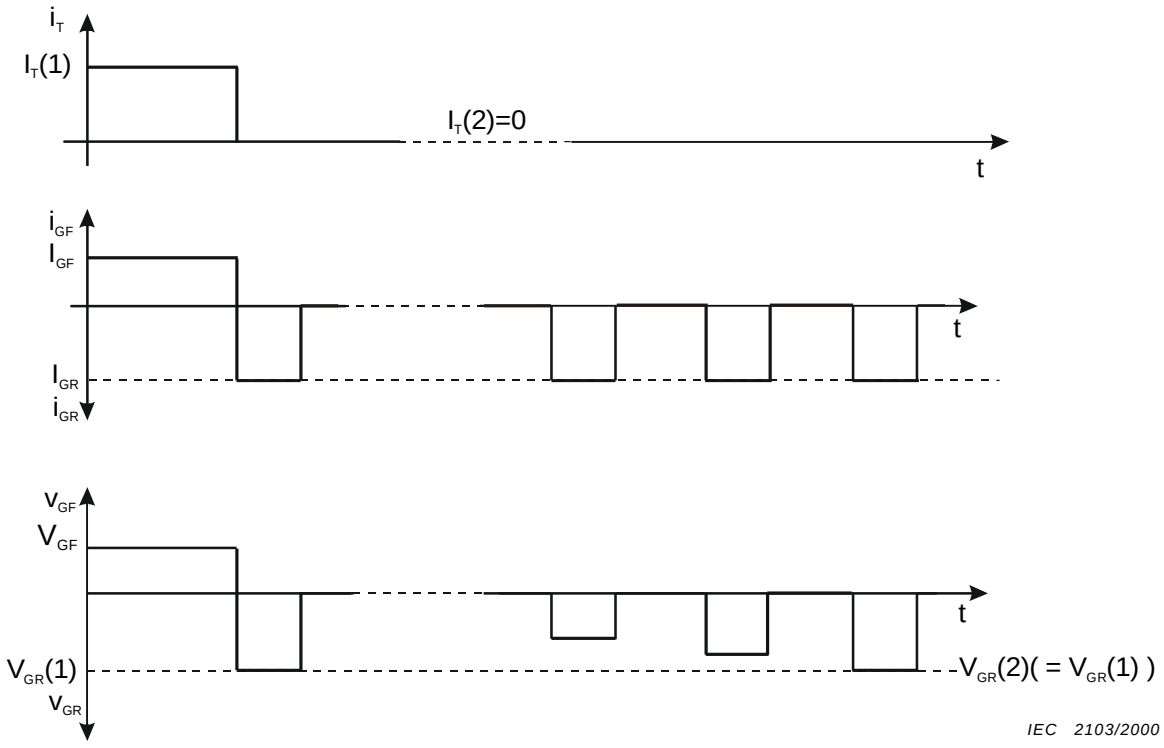


Figure 70 – Waveforms for measuring thermal resistance

Circuit description and requirements

G_1 heating current generator (I_T)

G_2 gate current generator

G_3 constant current pulse generator

I_T heating current generating the power loss P in the junction of T

S_1 electronic switch to interrupt heating current I_T

S_2 electronic switch to commutate the gate from generator G_2 to G_3

M measuring instrument to measure V_{GR}

W wattmeter to indicate the power loss P in the GTO thyristor caused by the heating current I_T

Precautions to be observed

There shall be no significant rise of the virtual junction temperature during the reference current pulse. See 9.2.5.1.

Measurement procedure

The GTO thyristor to be measured is mounted in such a way, that the reference point temperature can sufficiently be stabilized and measured as required in 9.2.1.

The measurement is carried out in three steps:

a) the reference point temperature is maintained at a lower value $T_r(1)$. The current $I_T(1)$ is turned on and the power P(1) warms up the junction until thermal equilibrium is reached. $T_r(1)$ and P(1) are recorded;

b) the current I_T is interrupted by opening switch S_1 ($I_T(2) = 0$). Simultaneously S_2 switches the gate from G_2 to G_3. The avalanche voltage $V_{GR}(1)$ is measured immediately after opening switch S_1;

c) the reference point temperature is increased until the avalanche voltage reaches the same value as before ($V_{GR}(2) = V_{GR}(1)$).

The reference-point temperature $T_r(2)$ is recorded. The thermal resistance R_{th} is calculated using the equation:

$$R_{th} = \frac{T_r(2) - T_r(1)}{P(1)}$$

9.2.5.3 Transient thermal impedance ($Z_{th}(t)$)

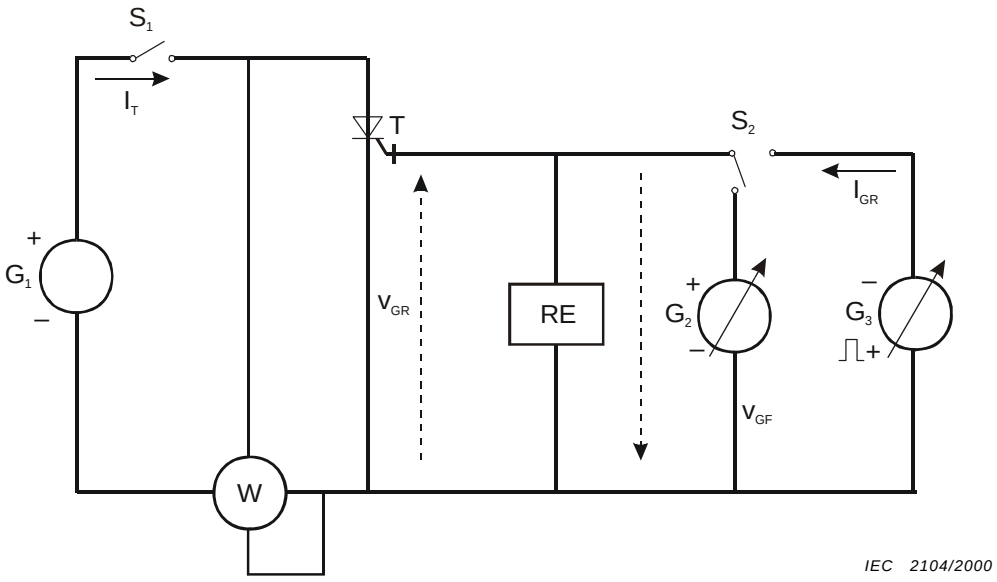
Purpose

To measure the transient thermal impedance of a gate turn-off thyristor between the virtual junction and a reference point.

Principle of the method

After applying the heating current and waiting until thermal equilibrium is established, the power loss in the device is recorded. The heating current is then interrupted and the avalanche voltage at the gate at a reference current pulse together with the reference-point temperature are recorded as a function of time.

By means of a calibration curve the recorded values of the avalanche voltage are converted to corresponding values of virtual junction temperature from which the transient thermal impedance is calculated.



T thyristor being measured

Figure 71 – Basic circuit diagram for the measurement of $Z_{th}(t)$ (method C)

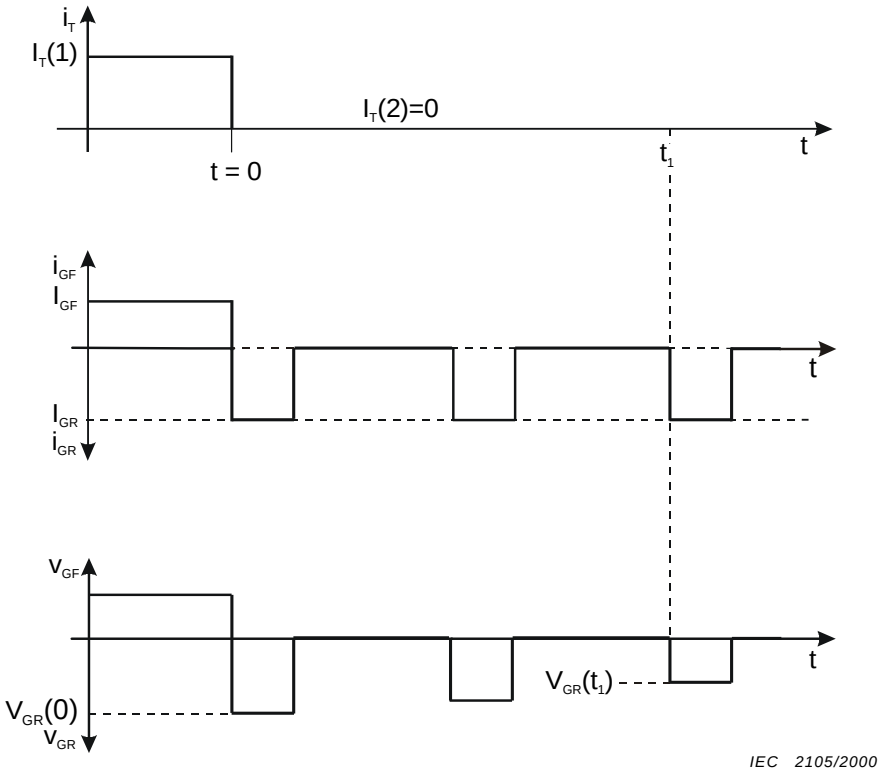


Figure 72 – Waveforms for measuring the transient thermal impedance of a gate turn-off thyristor

Circuit description and requirements

G_1 heating current generator (I_T)

G_2 gate current generator

G_3 constant current pulse generator

I_T heating current generating the power loss P in the junction of T

S_1 electronic switch to interrupt heating current I_T

S_2 electronic switch to commutate gate from generator G_2 to G_3

RE recording equipment, for example a transient recorder to record the avalanche voltage V_{GR} on the gate with its time variation on the reference current pulses

W wattmeter to indicate the power loss P in the GTO thyristor caused by the heating current I_T

Precautions to be observed

There shall be no significant rise of the virtual junction temperature during the reference current pulse. See 9.2.5.1.

Measurement procedure

The GTO to be measured is mounted in such a way that the reference point temperature can sufficiently be stabilized and measured as required in 9.2.1.

A calibration curve is prepared as described in 9.2.5.1.

For the measurement, the load current $I_T(1)$ is applied generating the power loss P(1) in the GTO being measured until thermal equilibrium is reached. The reference point temperature $T_r(1)$ is recorded.

At the time t = 0, the load current I_T is interrupted by opening switch S_1 to start the cooling period at zero power loss. Simultaneously with switch S_1, the switch S_2 switches the gate from G_2 to G_3. The avalanche voltage $V_{GR}(0)$ is measured immediately after opening switch S_1.

At the time t_1, the avalanche voltage $V_{GR}(t_1)$ is recorded together with the reference point temperature $T_r(t_1)$. Periodical recording during the cooling period is possible if the periodical heating by the reference current pulse can be tolerated.

For the calculation of the transient thermal impedance, the recorded values of $V_{GR}(0)$ and V_{GR} (t_1) are converted to the corresponding values of $T_j^*(0)$ and $T_j^*(t_1)$ by means of the calibration curve. The transient thermal impedance is calculated (see equation (21) in 9.2.4.1) as

$$Z_{th(j-r)}(t_1) = \frac{\left[T_j^*(0) - T_j^*(t_1)\right] - \left[T_r(0) - T_r(t_1)\right]}{P(1)}$$

9.2.6 Method D

Partial thermal resistances $R_{th(j-c)A}$ and $R_{th(j-c)K}$ of thyristors in disc-type housings (heat flow method)

Purpose

To measure the partial thermal resistance between the virtual junction and the anode side or cathode side of the case of a disc-type thyristor, $R_{th(j-c)A}$ or $R_{th(j-c)K}$ respectively.

Principles of the method

a) the heat flow from the anode side and the cathode side, respectively, of the disc-type housing to the appertaining heatsinks is measured by means of calibrated thermal resistors which are inserted between the contact plates of the thyristor to be measured and the heatsinks (r_A and r_K in figure 73a);

b) the two partial thermal resistances are measured in two steps:

   in the first step, the series thermal resistance $R_s = R_{th(j-c)A} + R_{th(j-c)K}$ is measured by applying externally a heat flow from the anode side to the cathode side of the housing (figure 73a);

   in the second step, a measured power is dissipated within the thyristor being measured (figure 73b).

   The power sharing to anode side and cathode side is measured, and from this and the known value of R_s the two partial thermal resistances can be calculated.

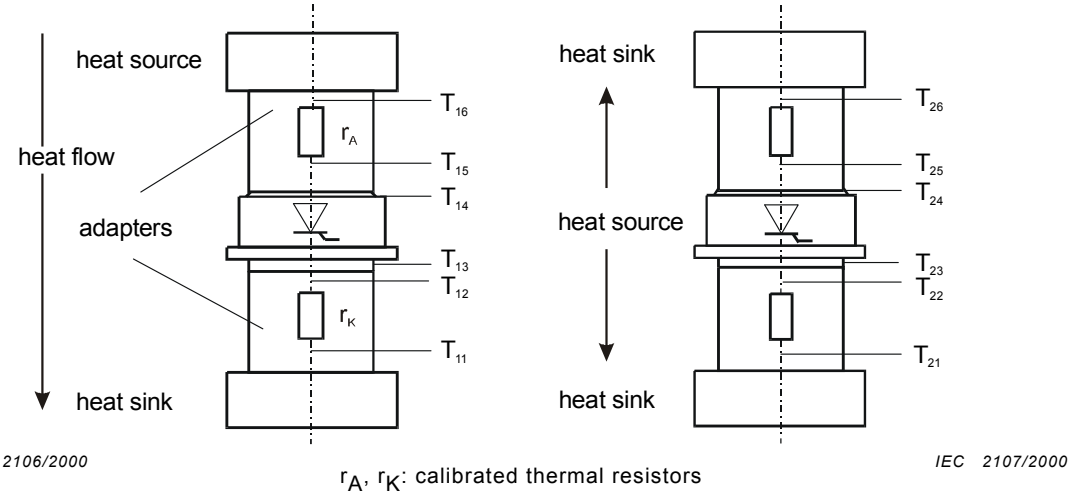


Figure 73a – Application of heat flow from anode to cathode side of housing

Figure 73b – Dissipation of measured power within thyristor

Figure 73 – Calibration and measurement arrangement for the heatflow method

Calibration of r_A and r_K

In principle, r_A and r_K could be calculated as

$$r_{A,K} = \frac{4d}{D^2 \pi \lambda}$$

where

D is the diameter of the cylindric adapters in centimetres;

d is the axial distance between the mounting points of the appertaining thermosensitive devices in centimetres;

λ is the thermal conductivity of the material of the adapter (W/cm·K).

However, there are some reasons to use this formula for estimations only:

– the material constant λ is not always known with sufficient exactitude; there are, for example, different kinds of industrial copper;

– there are unknown tolerances for the value “d” and of the diameter and sensitivity of the thermosensitive elements.

An exact calibration of the adapters is therefore recommended.

The calibration is performed in an arrangement as shown in figure 73b. A symmetrical electrical heating element is used as a heat source and the total electrical power “P” from the heating element is measured.

Both adapters as well as the heatsink arrangement, shall be identical, so that the power is equally dissipated on both sides. Then r_A and r_K follow from the measured differences in temperature:

$$r_A = \frac{2 \cdot (T_{25} - T_{26})}{P} \qquad r_K = \frac{2 \cdot (T_{22} - T_{21})}{P}$$

If a semiconductor device is used as a heating element, it shall be a thermally symmetrical device to avoid complications caused by asymmetrical heat flow. A relevant check can be made by turning over the heating element and calibrating r_A and r_K the same way as before. In case of different results, the mean values between the two measurements shall be taken.

During calibration and measurement the heating device or the device being measured shall have good thermal isolation, so that losses to the ambient air can be neglected (they are anyhow of the same order at calibration and measurement).

For the adaptors, Cu can be used. Be-Cu is also advantageous since it is harder and has lower values of λ.

Regarding the measurement of the temperatures of the anode and cathode sides of the device, thermocouples or resistance thermometers for surface measurements should preferably be used, positioned at the centre of the contact plates of the device being measured and making contact by means of a spring.

Another method is to measure the temperature at a small, defined distance in the centre beneath the front plane of the adapter. In this way, the additional thermal resistance resulting from that distance and the surface contact are included in the measured values of the partial resistance. For correction, a typical value of the added resistance is then subtracted from the measured values.

During repeated testing, the quality of the contact plates of the adapters shall periodically be checked.

Precautions to be observed

As mentioned under “calibration of r_A and r_K”, good thermal isolation is required.

Measurement procedure

The measurement is carried out in two steps:

a) A heat flow through the device being measured is maintained by means of a heating and cooling system as shown schematically in figure 73a.

After having reached thermal equilibrium the temperatures T_{11},T_{12},....,T_{16} of the two adapters are recorded. The heat flow on the anode and cathode side can then be calculated by means of the calibrated thermal resistances r_A and r_K as

$$P_{A1} = (T_{16} - T_{15}) / r_A \qquad P_{K1} = (T_{12} - T_{11}) / r_K$$

Due to the low losses between the position of r_A and r_K, P_{A1} will be slightly higher than P_{K1} and thermal series resistance

$$Rs = R_{th(j\text{-}c)A} + R_{th(j\text{-}c)K}$$

is calculated from the mean values of P_{A1} and P_{K1} as

$$R_S = 2\frac{T_{14} - T_{13}}{P_{A1} + P_{K1}}$$

b) A heat flow from both sides of the thyristor is caused by means of a direct current through the device being measured (see figure 73b).

After having reached thermal equilibrium, the temperatures T_{21}, T_{22},...., T_{26} on the two adapters are recorded.

The heat flow to both sides is calculated as

$$P_{A2} = (T_{25} - T_{26}) / r_A \qquad P_{K2} = (T_{22} - T_{21}) / r_k$$

With these values and T_{24} and T_{23} the virtual junction temperature and the partial thermal resistances can be calculated using the expressions

$$T_j = \frac{P_{A2}P_{K2}R_S + T_{23}P_{A2} + T_{24}P_{K2}}{P_{A2} + P_{K2}}$$

$R_{th(j\text{-}c)A} = (T_j - T_{24}) / P_{A2}$

$R_{th(j\text{-}c)K} = (T_j - T_{23}) / P_{K2}$

From the two partial thermal resistances a combined thermal resistance $R_{th(j\text{-}c)}$ can be calculated:

$$R_{th(j-c)} = \frac{R_{th(j-c)A} - R_{th(j-c)K}}{R_{th(j-c)A} + R_{th(j-c)K}}$$

However, this value is of practical importance only under the assumption that the heatsink temperatures on both sides are approximately the same.

9.3 Verification test methods for ratings (limiting values)

9.3.1 Non-repetitive peak reverse voltage (V_{RSM})

Purpose

To verify the non-repetitive peak reverse voltage rating of a thyristor under specified conditions.

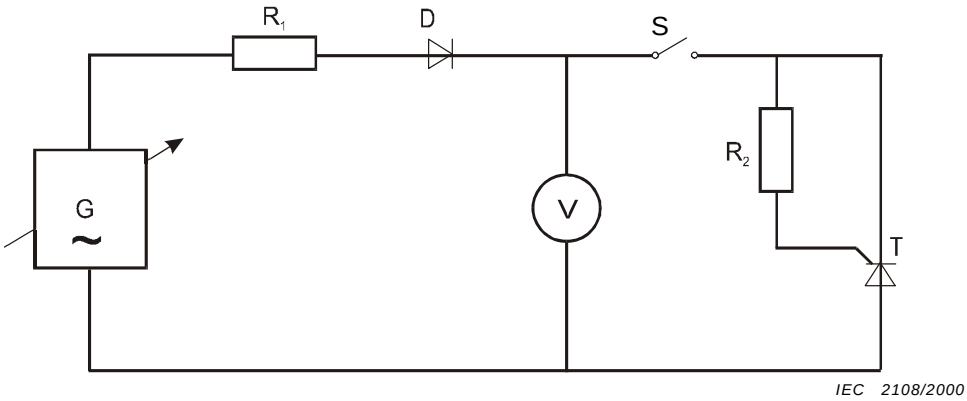


Figure 74 – Circuit diagram for measuring non-repetitive peak reverse voltage rating

Circuit description and requirements

D diode to provide negative half cycles, so that only the reverse characteristic of the thyristor is tested

G alternating voltage source

S electromechanical or electronic switch (with a conduction angle of approximately 180°) which applies the source voltage to the thyristor under test for the half cycle in the reverse direction

T thyristor under test

V peak reading instrument

Test procedure

With bias conditions set to zero, the thyristor under test is inserted into the test socket.

Switch S is opened and the a.c. source voltage is increased to the specified value of non-repetitive peak reverse voltage.

The specified temperature conditions are checked.

The specified non-repetitive peak reverse voltage is applied by closing switch S for approximately 180° during the reverse half cycle.

NOTE The repetition rate should be such that the thermal effect of one pulse will have completely disappeared before the next pulse arrives.

Proof of the ability of the thyristor to withstand the non-repetitive peak reverse voltage rating is obtained from the post-test measurements.

Specified conditions

The values of the following conditions shall be stated:

a) non-repetitive peak reverse voltage;

b) gate-cathode resistor;

c) ambient, case or reference point temperature;

d) duration of the half cycle pulse;

e) number of pulses and repetition rate;

f) post-test measurement limits.

9.3.2 Non-repetitive peak off-state voltage (V_{DSM})

Purpose

To verify the non-repetitive peak off-state voltage rating of a thyristor under specified conditions.

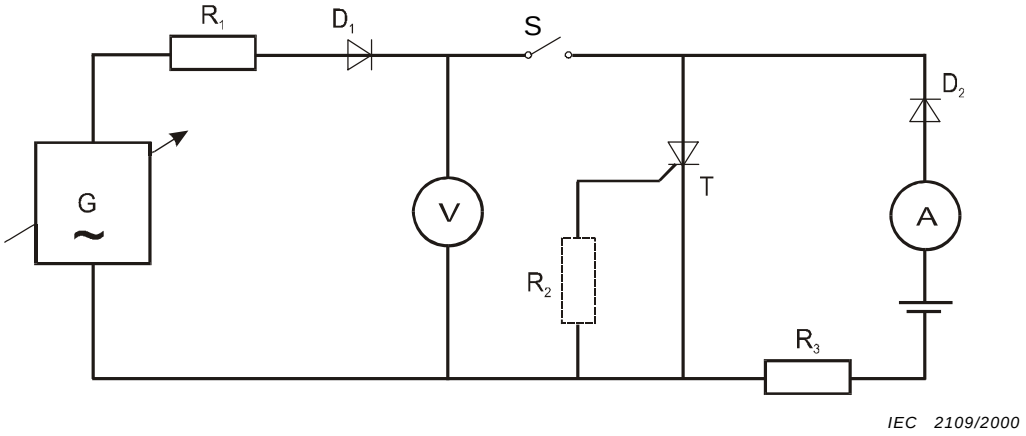


Figure 75 – Circuit diagram for measuring non-repetitive peak off-state voltage rating

Circuit description and requirements

D_1 diode to provide positive half cycles, so that only the off-state characteristic of the thyristor is tested

G alternating voltage source

R_1 and R_3 protective resistors

NOTE 1 R_2 is only to be used if specified.

S electromechanical or electronic switch (with a conduction angle of approximately 180°) which applies the source voltage to the thyristor under test for one half cycle in the off-state condition

T thyristor under test

V peak reading voltmeter

The low voltage d.c. source, ammeter A and limiting resistor R_3 are used to verify that the thyristor has not reached breakover and is not in the on-state condition. The ammeter and the d.c. source can be replaced by an indicating instrument, e.g. an oscilloscope.

Measurement procedure

With the a.c. source set to zero, the thyristor under test is inserted into the test socket.

Switch S is opened and the a.c. source voltage is increased to the specified value of non-repetitive peak off-state voltage.

The specified temperature conditions are checked.

The specified non-repetitive peak off-state voltage is then applied to the thyristor under test by closing switch S for approximately 180° during the off-state half cycle.

NOTE 2 The repetition rate should be such that the thermal effect of one pulse will have completely disappeared before the next pulse arrives.

Proof of the ability of the thyristor to withstand the non-repetitive peak off-state voltage rating is obtained from the post-test measurement.

Specified conditions

The values of the following conditions shall be stated:

a) non-repetitive peak off-state voltage;
b) gate-cathode resistor R_2;
c) ambient, case or reference point temperature;
d) duration of the half cycle pulse;
e) number of pulses and repetition rate;
f) post-test measurement limits.

9.3.3 Surge (non-repetitive) on-state current (I_{TSM})

Purpose

To verify the surge (non-repetitive) on-state current rating of a thyristor under specified conditions.

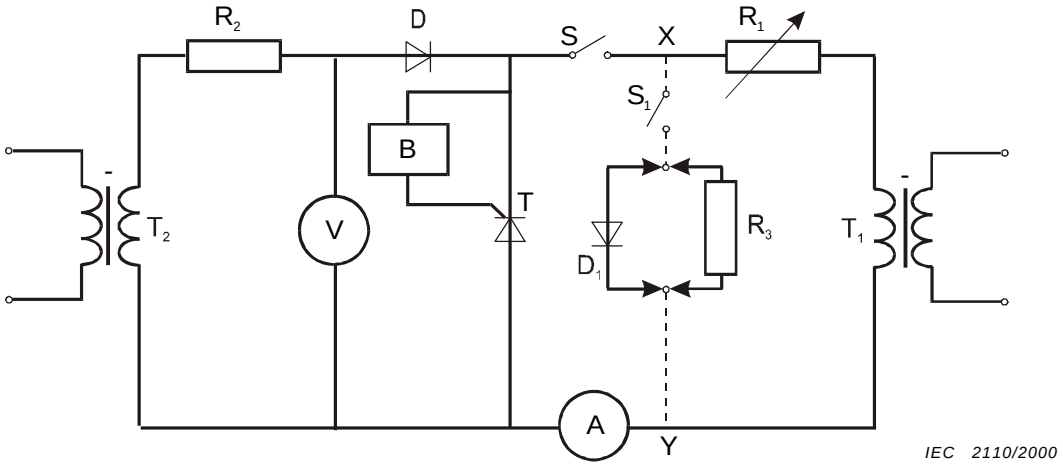


Figure 76 – Circuit diagram for measuring surge (non-repetitive) on-state current rating

Circuit description and requirements

A peak reading instrument (e.g. ammeter or oscilloscope)

B gate bias circuit

D diode to block the forward voltage supplied by transformer T_2

R_1 surge current setting resistor which shall be large compared with the forward resistance of diode D_1, when present (see note below)

R_2 protective resistor whose value shall be as small as practicable

S electromechanical or electronic switch with a conduction angle of approximately 180° during the on-state (surge) half cycle

T thyristor under test

T_1 high-current, low-voltage transformer supplying through S the on-state (surge) half cycle. The current waveshape shall be essentially a half sine wave of approximately 10 ms (or 8,3 ms) duration, with a repetition rate of approximately 50 (or 60) pulses per second.

T2 low-current high-voltage transformer supplying through diode D the reverse half cycle and, if fed from a separate source, its phase shall be the same as that feeding T_1. The voltage form shall be essentially a half sine wave.

V peak reading instrument (e.g. voltmeter or oscilloscope)

NOTE If desirable, either a diode D_1 in series with a switch S_1, or a resistor R_3 in series with a switch S_1 may be inserted between points X and Y. These circuits are not mandatory. D_1 is a current balancing diode having approximately the same forward resistance as the on-state resistance of the thyristor under test.

If a resistor R_3 is used, it should have the same resistance as the on-state resistance of the thyristor under test.

S_1 is an electromechanical or electronic switch with a conduction angle of approximately 180° during the reverse half cycle of transformer T_1.

Test procedure

The voltage and current sources are set to zero.

The thyristor is inserted into the test socket in accordance with its polarity marking and the temperature conditions are checked.

The peak reverse voltage, measured on peak reading instrument V, is adjusted to the specified value.

The surge on-state current, measured on peak reading instrument A, is set to the specified value by adjustment of R_1.

The thyristor under test is then triggered for the specified number of applications of surge on-state current. Care should be taken to avoid applying the triggering signal during the reverse half cycle.

Proof of the ability of the thyristor to withstand the surge on-state current rating is obtained from the post-test measurements.

Specified conditions

The values of the following conditions shall be stated:

a) peak reverse voltage;

b) surge (non-repetitive) on-state current;

c) maximum impedance of the reverse voltage source;

d) gate bias conditions: source voltage and source resistance;

e) number of cycles per surge, number of surges and repetition rate;

f) ambient, case or reference point temperature;

g) post-test measurement limits.

9.3.4 On-state current ratings of fast-switching thyristors

Purpose

To verify the maximum rated value of the on-state current of a fast-switching thyristor under specified conditions.

NOTE The circuit commutated turn-off time of the thyristor under test is used as an indication of the ability of the thyristor to carry this current.

Test circuit

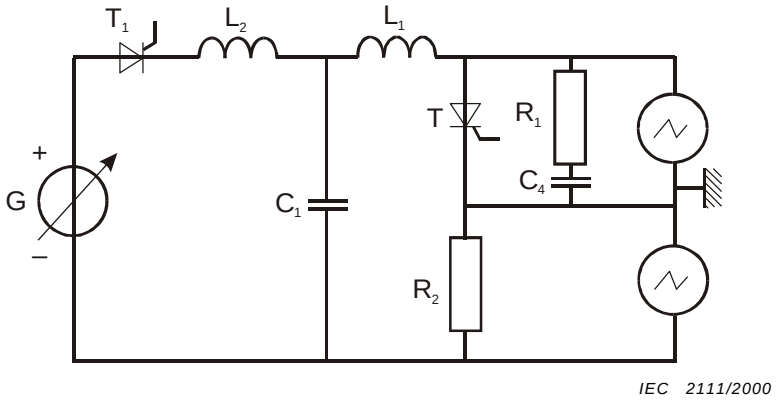
Test methods are given for the following operating conditions:

a) sinusoidal on-state current with reverse voltage applied (9.3.4.1);
b) sinusoidal on-state current with reverse voltage suppressed (9.3.4.2);
c) trapezoidal on-state current with reverse voltage applied (9.3.4.3);
d) trapezoidal on-state current with reverse voltage suppressed (9.3.4.4).

Throughout these test methods, the test circuit hold-off interval (t_H) shall be made equal to the specified maximum value of circuit committed turn-off time (t_q).

If a heatsink is connected to the anode of the thyristor under test, it is permissible to reverse the polarity of all supplies, and the direction of all thyristors and diodes, in order to earth this heatsink.

9.3.4.1 Sinusoidal on-state current with reverse voltage applied



T thyristor under test

Figure 77a – Basic circuit diagram for measuring sinusoidal on-state current with reverse voltage

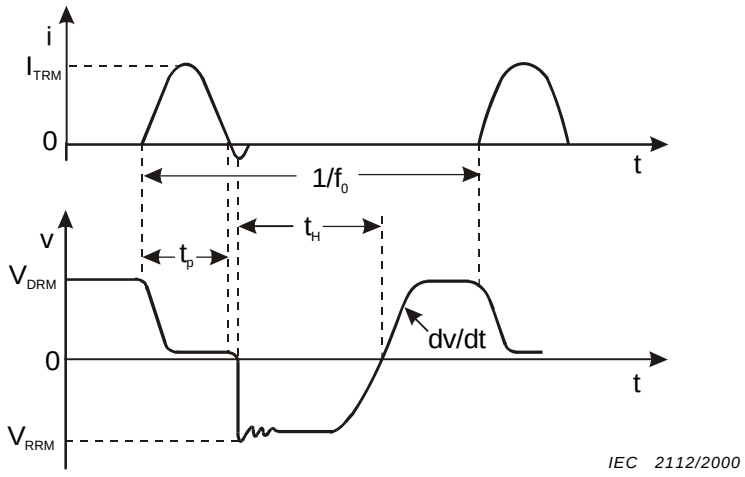


Figure 77b – Waveforms produced when measuring sinusoidal on-state current with reverse voltage

Figure 77 – Basic circuit and test waveforms for sinusoidal on-state current with reverse voltage

Circuit description and requirements

G d.c. source of low impedance

L_1, C_1 resonant circuit determining the on-state current half sine wave pulse duration t_p and amplitude I_{TRM}:

$$t_p = \pi\sqrt{L_1 C_1} \qquad I_{TRM} = \frac{V_{DRM}}{\sqrt{\frac{L_1}{C_1}}}$$

L_2, C_1 resonant circuit set to give the specified rate of rise of the reapplied off-state voltage (together with R_1, C_4)

NOTE 1 The lowest possible hold-off interval is

$$t_H\ (\text{min}) = \frac{\pi}{2}\sqrt{L_2 C_1}$$

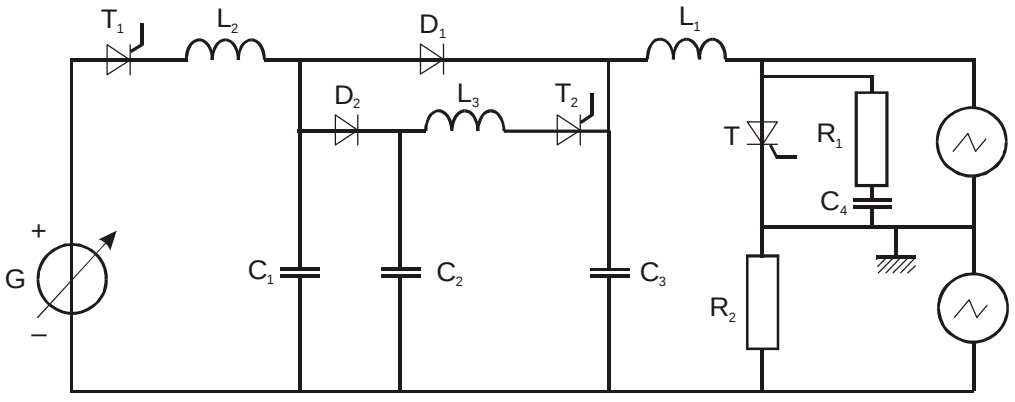
NOTE 2 The off-state voltage V_{DRM} across the thyristor to be measured (see figure 77) is equal to the peak voltage across C_1 and may be up to 10 times the voltage of the d.c. source, depending on the circuit elements. Care shall be taken not to exceed the specified V_{DRM} value.

R_1, C_4 damping network for protecting the thyristor under test T. A similar RC damping network may be used for protecting thyristor T_1

T_1 auxiliary thyristor; T_1 is usually required to have a much higher elevated frequency current rating than the thyristor under test

R_2 current measuring resistor

C_1 is charged from the d.c. source by triggering T_1. After T_1 has turned off, T is triggered; this discharges C_1 via L_1 and T, producing a half sine wave current pulse of duration t_p. C_1 then recharges in the reverse direction. After a suitable time, T_1 is triggered again, causing the voltage across the thyristor T to change from the negative level to a positive level at the specified dv/dt. This time is adjusted to give the required hold-off time interval. At the same time, the voltage across C_1 is further charged from G and changes polarity. Repetition of this cycle builds up the voltage across C_1 to the required level (about 10 times the d.c. source voltage).



IEC 2113/2000

T thyristor under test

Figure 78 – Extended circuit diagram for measuring sinusoidal on-state current with reverse voltage

Circuit description and requirements

The test waveform and requirements are the same as for the basic circuit of figure 77 except that

$$t_H \text{ (min)} = \frac{\pi}{2}\sqrt{L_3 C_3}\ .$$

By adding C_2, C_3, T_2, L_3, D_1, D_2, the test circuit is more flexible and capable of being set to give a higher dv/dt in order to test thyristors with shorter circuit commutated turn-off times. The capacity of C_1 and C_2 is at least 10 times the capacity of C_3. D_1 and D_2 decouple C_2 and C_3 from C_1.

C_1, C_2, C_3 are charged from the d.c. source through T_1 and T_2. When T is triggered, C_1 and C_3 discharge via L_1 and T, producing a half sine wave current and are recharged in the reverse direction. After a suitable time, T_2 is triggered causing a voltage rise from the reverse direction to the forward direction of T by transfer of charge from C_2 to C_3 ($C_2 >> C_3$). This time is adjusted to give the specified hold-off interval (t_H). For the next test cycle, C_1, C_2 and C_3 are recharged from the d.c. source by triggering T_1. The voltages of C_1, C_2 and C_3 are stepped up to about 10 times the voltage of the d.c. source by the repetition of the test cycles.

Test procedure

The reference point temperature is set to the specified value.

The triggering sources for the thyristors T and T_1 are adjusted to give the specified repetition frequency (f_0) and hold-off interval (t_H). Source G is adjusted to obtain the specified on-state current.

If the thyristor under test does not withstand its specified repetitive peak off-state voltage it has failed the test.

Specified conditions

a) reference point temperature;

b) repetition frequency (f_0);

c) off-state voltage (V_{DRM});

d) reverse voltage, where appropriate;

e) on-state current pulse duration (t_p) and amplitude (I_{TRM});

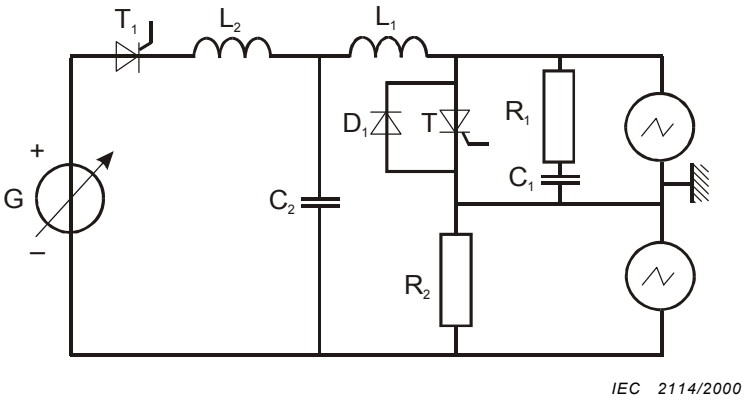
f) rate of rise of the re-applied off-state voltage (dv/dt);

g) hold-off interval (t_H) (this shall equal the specified maximum circuit commuted turn-off time);

h) triggering circuit conditions;

i) RC damping network (R_1, C_4).

9.3.4.2 Sinusoidal on-state current with reverse voltage suppressed



T thyristor under test

Figure 79a – Basic circuit diagram for measuring sinusoidal on-state current with reverse voltage suppressed

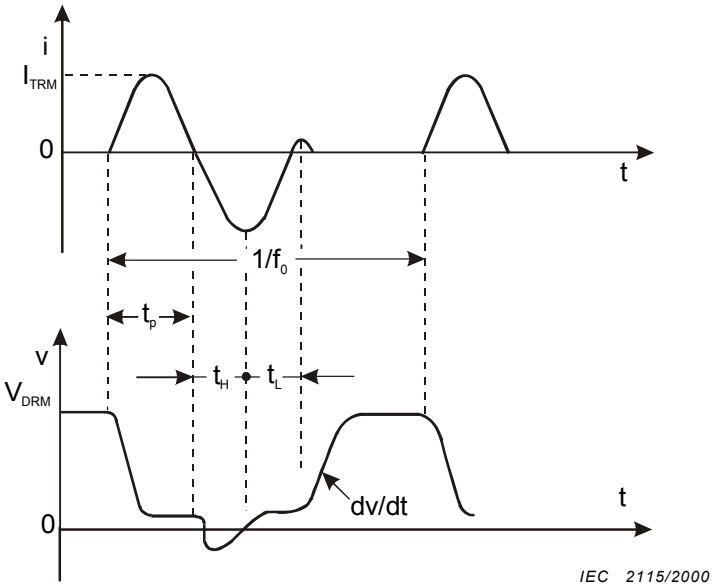


Figure 79b – Waveforms produced when measuring sinusoidal on-state current with reverse voltage suppressed

Figure 79 – Basic circuit and test waveforms for sinusoidal on-state current with reverse voltage suppressed

NOTE The voltage across the thyristor may be positive for time t_L due to the inductance of the T, D_1 loop. This must be kept to a minimum to reduce this voltage as much as possible. The negative part of the current waveform represents the current through diode D_1.

Circuit description and requirements

G d.c. source of low impedance

L_1, C_2 resonant circuit determining the on-state current half sine wave pulse duration t_p and amplitude I_{TRM} and the hold-off interval t_H:

$$t_p = \sqrt{L_1 C_2} \qquad I_{TRM} = \frac{V_{DRM}}{\sqrt{\frac{L_1}{C_2}}}$$

The value of C_2 should be adjusted to give the required hold-off interval.

This will lie between

$$t_H\,(\min) \approx \frac{\pi}{2}\sqrt{L_1 C_2} \qquad \text{and} \qquad t_H\,(\max) = \pi\sqrt{L_1 C_2}$$

NOTE V_{DRM} is approximately equal to the d.c. source voltage (G).

R_1, C_1 damping network set to give the specified rate of rise of the re-applied off-state voltage. A similar network may be used to protect T_1

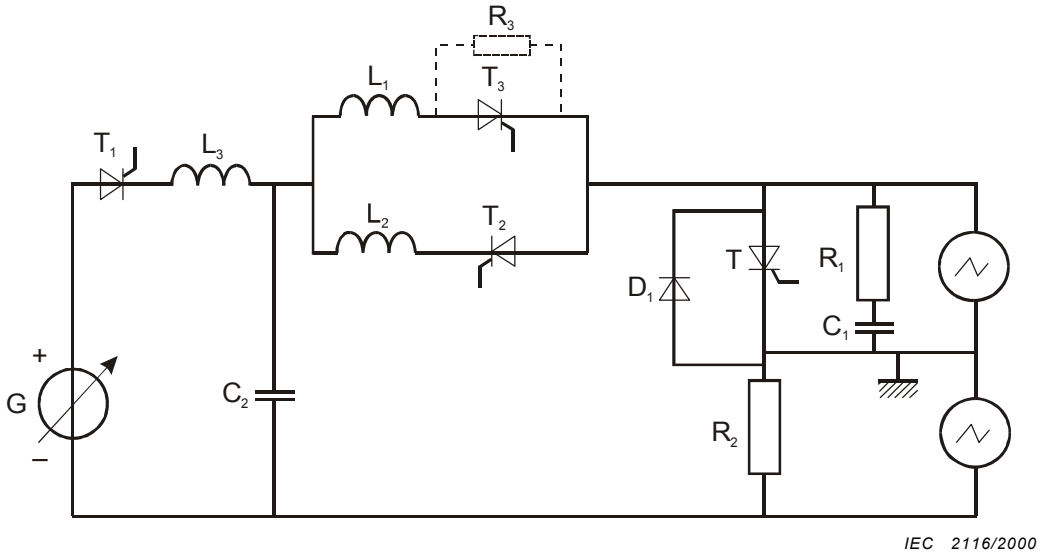
R_2 current measuring resistor

D_1 diode for suppressing reverse voltage

T_1 auxiliary thyristor

L_2 protection inductor for di/dt of T_1

C_2 charged by triggering T_1. After T_1 has turned off, T is triggered. C_2 discharges via L_1 producing a half sine wave current. When T has recovered, the energy swings back to C_2 via D_1, and the effective loss of charge in C_2 is replaced from the d.c. source by triggering T_1.



T thyristor under test

Figure 80 – Extended circuit diagram for measuring sinusoidal on-state current with reverse voltage suppressed

Circuit description and requirements

The test waveform and requirements are the same as for the basic circuit given in figure 77 except that

$$t_H\,(\min) = \frac{\pi}{2}\sqrt{L_2 C_2}$$

R_3 is a by-pass resistor if required.

T_3 is triggered at the same time as T.

By adding L_2, T_2 and T_3, the test circuit is more flexible.

The hold-off interval (t_H) may be varied independently of the pulse duration (t_p) by introducing a delay time between the end of the current pulse and the triggering of T_2, and by using an inductance L_2 that is different from L_1.

It is recommended that the diode D_1 be a fast turn-on diode to decrease the reverse recovery power dissipation in the thyristor under test (T).

Test procedure

The temperature is set to the specified value.

The triggering sources for the thyristors T and T_1 are adjusted to give the specified repetition frequency (f_0) and the hold-off interval (t_H). Source G is adjusted to obtain the specified on-state current.

If the thyristor under test does not withstand its specified repetitive peak off-state voltage, it has failed the test.

Specified conditions

a) reference point temperature;

b) repetition frequency (f_0);

c) off-state voltage (V_{DRM});

d) on-state current pulse duration (t_p) and amplitude (I_{TRM});

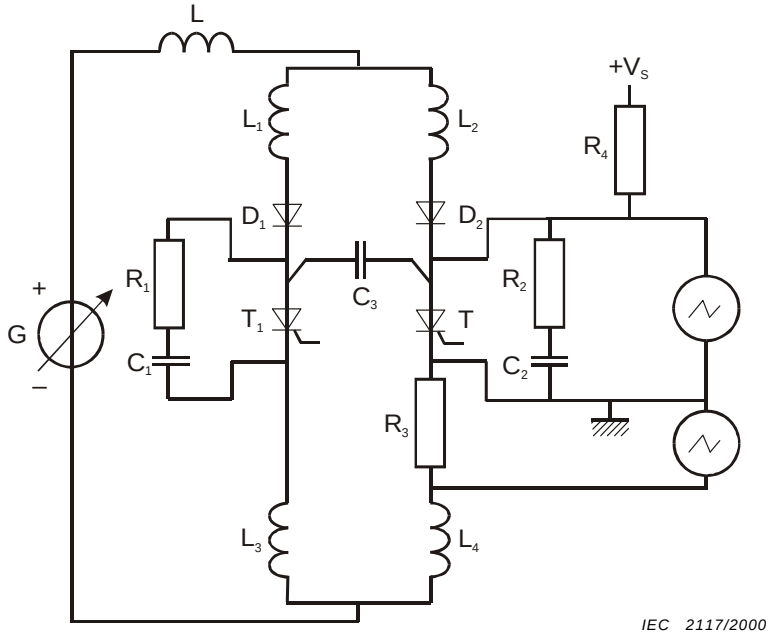
e) rate of rise of the re-applied off-state voltage (dv/dt);

f) hold-off interval (t_H) (this shall be equal to the specified maximum circuit commutated turn-off time);

g) triggering circuit conditions;

h) RC damping network (R_1, C_1).

9.3.4.3 Trapezoidal on-state current with reverse voltage applied



T thyristor under test

Figure 81a – Circuit diagram for measuring trapezoidal on-state current with reverse voltage applied

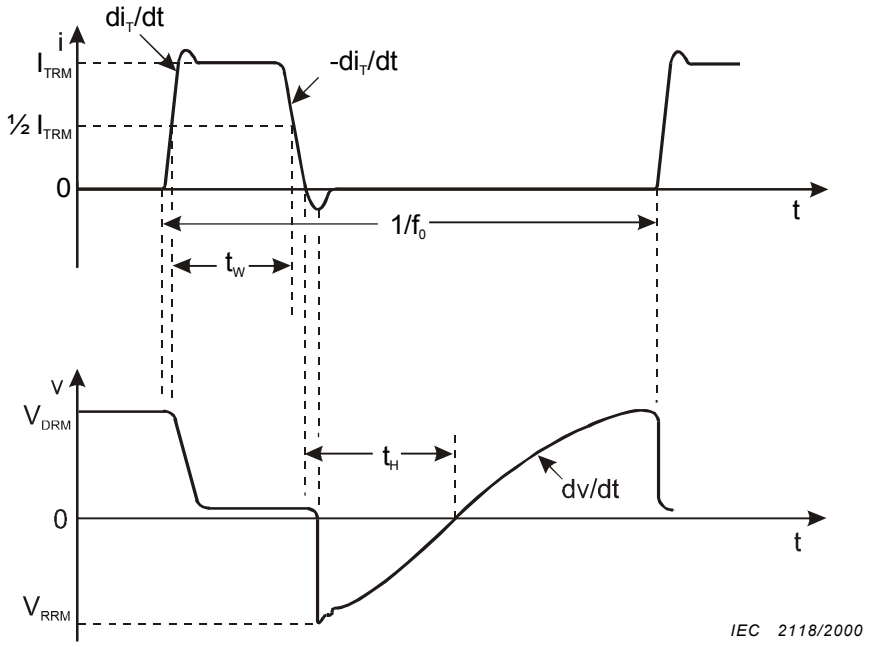


Figure 81b – Test waveforms produced when measuring trapezoidal on-state current with reverse voltage applied

Figure 81 – Basic circuit and test waveforms for trapezoidal on-state current with reverse voltage applied

Circuit description and requirements

G, L	direct high-current source
V_S	direct high-voltage source (for starting purposes if required)
C_3	commutation capacitor
L_1, L_2	inductances determining the hold-off interval t_H: $t_H \approx \sqrt{C_3 (L_1 + L_2)}$
L_3, L_4	inductances determining the rate of rise of on-state current in the thyristor
D_1, D_2	blocking diodes
T_1	auxiliary thyristor
R_1, C_1 R_2, C_2	damping networks for protecting the thyristors
R_3	current-measuring resistor or current probe
R_4	current-limiting resistor

The two thyristors, T and T_1, conduct the current alternately. Initially, T_1 is triggered, and C_3 is charged to a high voltage approaching V_{DRM} by source V_S via R_4. When T is triggered, the charge on C_3 reverse biases T_1, thus causing it to turn off. Current through L_1 then re-charges C_3 in the opposite direction, until T_1 is triggered to reverse bias T and cause it to turn off. C_3 is then charged via L_2 and D_2, giving the rise of voltage (dv/dt) across T.

By repeating the commutation, a step-up of voltage is generated in the oscillation loop L_1, L_2 and C_3 until a voltage is reached which is much higher than the voltage of the source G. Source V_S may be then disconnected. Approximately

$$V_{DRM} = V_{RRM} = I_{TRM} \sqrt{\frac{L_1 + L_2}{C_3}}$$

The inductor L ensures a constant current in the circuit.

The on-state current pulse duration in the thyristor under test may be varied independently of the repetition frequency by varying the conduction period of T_1. The rate of rise of on-state current is approximately given by

$$\frac{di_T}{dt} = \frac{V_{DRM}}{L_3 + L_4}$$

Test procedure

The temperature is set to the specified value.

Thyristor T_1 is triggered, and source G is set to give a suitable low value of current. C_3 is charged for starting from source V_S. The triggering sources for T and T_1 are adjusted to the specified repetition frequency f_0 and on-state current pulse duration t_w. The pulse operation is started by triggering T.

Source V_S is disconnected and source G is re-adjusted to obtain the specified on-state current.

If the thyristor under test does not withstand its specified repetitive peak off-state voltage, it has failed the test.

Specified conditions

a) reference point temperature;

b) repetition frequency (f_0);

c) off-state and reverse voltages (V_{DRM} and V_{RRM});

d) on-state current pulse duration (t_w) and amplitude (I_{TRM});

e) rate of rise and fall of on-state current (di_T/dt and $-di_T/dt$);

f) hold-off interval (t_H) (this shall be equal to the specified maximum circuit commutated turn-off time);

g) triggering circuit conditions;

h) RC-damping network (R_1, C_1).

9.3.4.4 Trapezoidal on-state current with reverse voltage suppressed

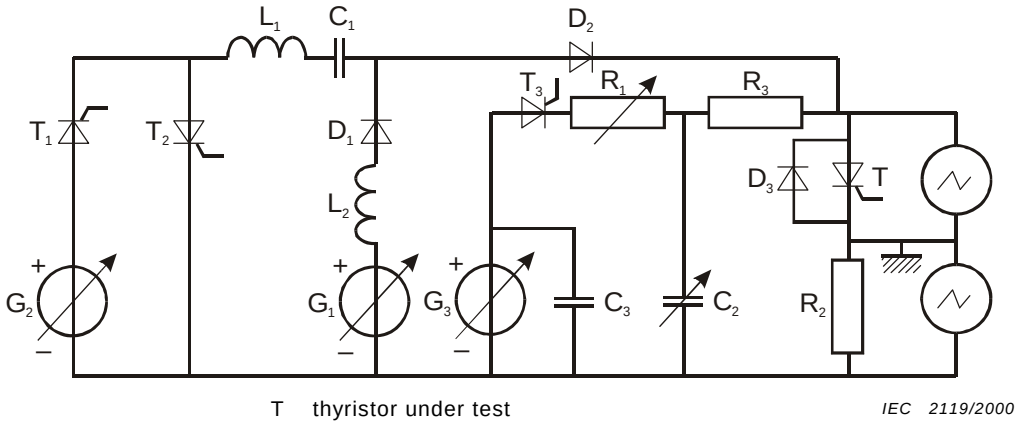


Figure 82a – Circuit diagram for measuring trapezoidal on-state current with reverse voltage suppressed

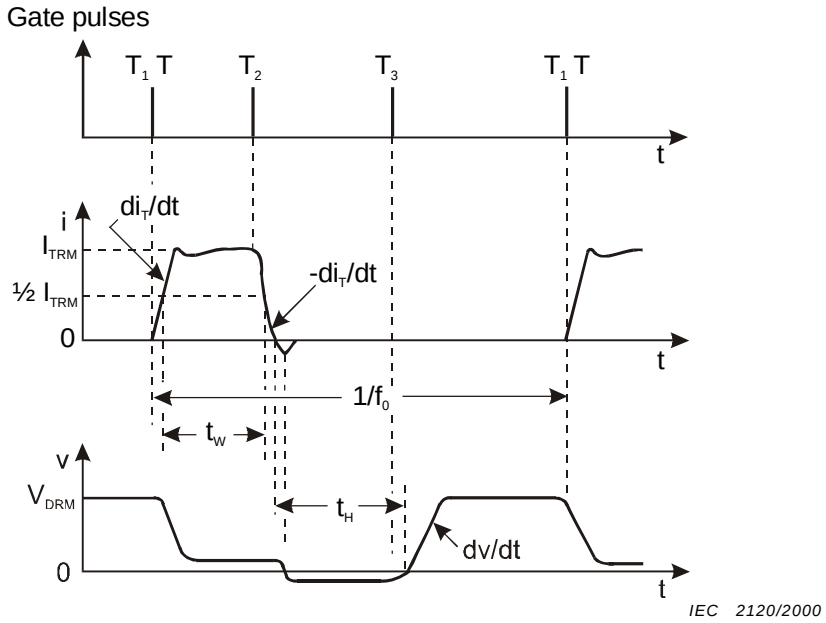


Figure 82b – Test waveforms produced when measuring trapezoidal on-state current with reverse voltage suppressed

Figure 82 – Basic circuit and test waveforms for trapezoidal on-state current with reverse voltage suppressed

Circuit description and requirements

G_1 low-impedance d.c. source: V_1

G_2 d.c. source: $V_2 > V_1$

G_3 high-impedance d.c. source: V_3 = off-state voltage V_{DRM}

C_1 commutating capacitor

C_3 storage capacitor for G_3 supply

R_1, C_2 dv/dt network

D_1, D_2 blocking diodes

NOTE 1 The recovery time of D_2 must be less than the turn-off time, but longer than the recovery time of the thyristor under test.

D_3 diode for suppressing reverse voltage

R_2 current-measuring resistor or current probe

R_3 protecting resistor if the thyristor under test fails the reapplied voltage

T_1 thyristor for charging the commutating circuit

T_2 thyristor for discharging the commutating circuit

T_3 thyristor for re-application of the forward voltage

L_1 commutating inductor

L_2 inductor to determine the rate the rise of on-state current di_T/dt

$$\pi\sqrt{C_1 L_1} > 2t_H \quad (22)$$

$$dv/dt = V_3/R_1C_2 \quad (23)$$

$$-di_T/dt = V_2/L_1 \quad (24)$$

Assume that the circuit is in the quiescent state, then T_1 and T are triggered simultaneously.

The independently adjustable load current flows through the path G_1, L_2, D_1, D_2, T and R_2 and at the same time C_1 is charged to the polarity shown through the path G_2, T_1, L_1, C_1, D_2, T and R_2. When C_1 is fully charged, T_1 ceases conduction.

At a later time, T_2 is triggered, the load current is shunted to the path G_1, L_2, D_1, C_1, L_1 and T_2. The voltage across C_1 is applied across D_2 in the reverse direction, voltage across T is suppressed by diode D_3.

When C_1 is charged in the polarity opposite to that shown and L_1 is discharged, T_2 ceases conduction.

When T_3 is triggered, the voltage initially across C_3 from source G_3 is applied to the thyristor under test and the damping circuit R_1C_2.

NOTE 2 Provided that the condition of equation (22) is met, the hold-off interval t_H will be determined by the triggering time of T_3.

Test procedure

The temperature is set to the specified value and the triggering circuits are switched on.

The forward current magnitude is set to a low value by adjusting G_1, the pulse duration is determined by the triggering of T_2.

The magnitude of the re-applied forward voltage is set by G_3, and the re-applied dv/dt is determined by R_1C_2.

The hold-off interval t_H is set to the value of the specified maximum circuit commutated turn-off time of the thyristor under test; the on-state current and operating frequency are adjusted to the specified values.

If the thyristor under test does not withstand its specified repetitive peak off-state voltage, it has failed the test.

Specified conditions

a) reference point temperature;

b) repetition frequency (f_0);

c) off-state voltage (V_{DRM});

d) on-state current pulse duration (t_w) and amplitude (I_{TRM});

e) rate of rise and fall of on-state current (di_T/dt and $-di_T/dt$);

f) hold-off interval (t_H) (this shall equal the specified maximum circuit commutated turn-off time);

g) rate of rise of the re-applied off-state voltage (dv/dt);

h) triggering circuit conditions.

9.3.5 Critical rate of rise of on-state current (di/dt)

Purpose

To verify the critical rate of rise of on-state current rating of a thyristor under specified conditions.

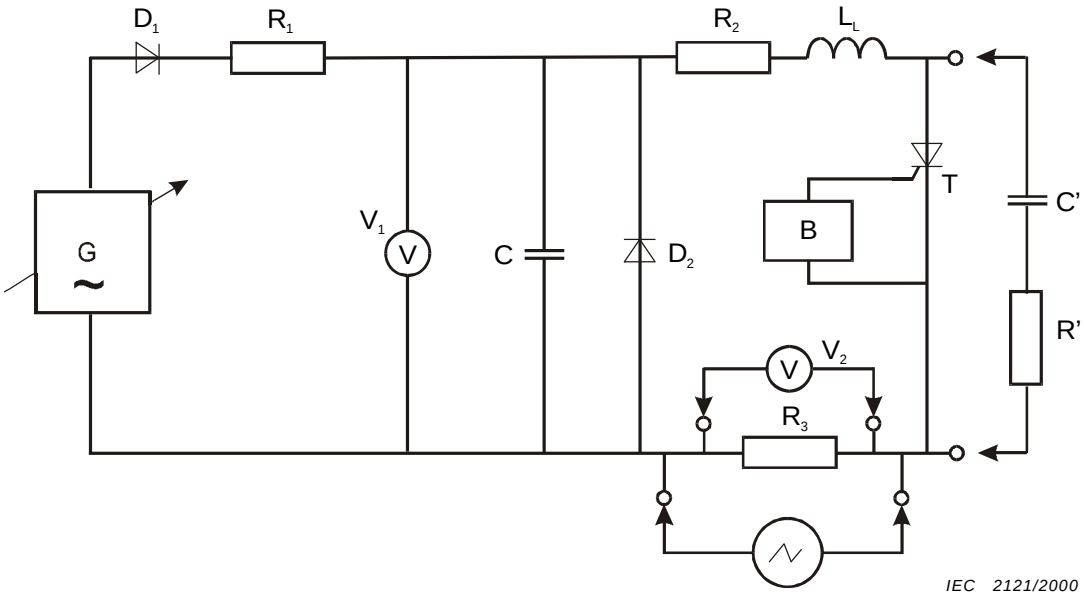


Figure 83 – Circuit diagram for measuring critical rate of rise of on-state current

Circuit description and requirements

B	gate-triggering source
G	alternating voltage source
D_2	diode which protects the thyristor under test from excessive reverse voltage which might arise from resonance effects
R_1 and D_1	are chosen so that the capacitor C has time to charge fully before each operation
R_3	calibrated non-inductive current sensing resistor
T	thyristor under test
V_1	high resistance voltmeter
V_2	peak reading voltmeter

To obtain the required rate of rise of on-state current of thyristor under test T, R_2, C and L are chosen such that their values are approximately related to the test voltage V_{DM}, current amplitude I_{TM} and time t_1 as follows:

$$C = 5{,}6\frac{I_{TM} \cdot t_1}{V_{DM}}$$

$$L = 1{,}7\frac{V_{DM} \cdot t_1}{I_{TM}}$$

$$R_2 = 0{,}55\frac{V_{DM}}{I_{TM}}$$

where

V_{DM} is the peak off-state voltage and

$$\frac{di}{dt} = \frac{0{,}5 I_{TM}}{t_1}$$

t_1 is defined in figure 84.

R_2 is used to damp the oscillatory waveforms. In the case of high-power devices it can consist of the distributed resistances of the circuit elements only. In that case it is assumed that R_2 can be neglected and the formulae in the note can be used.

NOTE For high-power devices, where R_2 is deleted, C and L are chosen such that their values are approximately related to the test voltage V_{DM}, current magnitude I_{TM} and time t_1 as follows:

$$C = 1{,}91\frac{I_{TM} \cdot t_1}{V_{DM}}$$

and

$$L = 1{,}91\frac{V_{DM} \cdot t_1}{I_{TM}}$$

R' and C' are chosen in accordance with the application of the thyristor under test and might be deleted where appropriate.

Final adjustments are made to L and C to ensure that the peak on-state current measured on voltmeter V_2 and the rate of rise of on-state current di/dt measured on the oscilloscope are as specified.

It is recommended that a damped sine wave be used as the on-state current waveform as shown in figure 84.

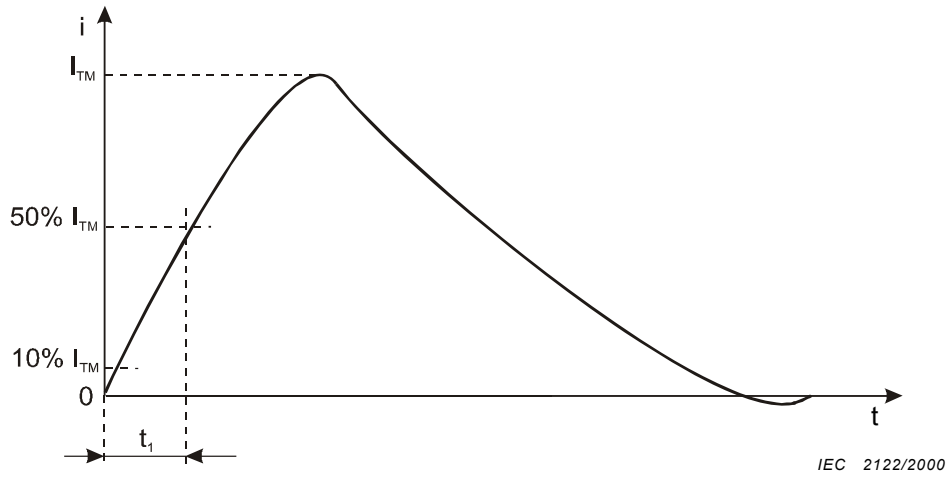


Figure 84 – On-state current waveform for di/dt rating

Zero time is determined by the intersection with the time axis of the straight line passing through the 10 % and 50 % test current points.

With this waveform, the recommended method of assigning a numerical value to di/dt is as follows:

$$\frac{di}{dt} = \frac{I_{TM}}{2t_1}$$

where

$t_1 \geq 1$ µs;

$I_{TM} \geq$ twice the mean on-state current rating.

Measurement procedure

The alternating voltage source is set to zero. Care should be taken to ensure that the capacitor C is fully discharged. The thyristor under test is inserted into the test socket and the temperature is set to the specified value.

The source voltage is set to give a peak voltage equal to the specified off-state voltage V_{DM} as shown by voltmeter V_1 when the capacitor C is fully charged.

The thyristor under test is triggered and capacitor C discharges through L and the thyristor.

The repetition rate is controlled by the gate triggering source and should be as specified. Care shall be taken that the gate trigger pulse occurs during the negative half cycle of the alternating voltage source.

Proof of the ability of the thyristor to withstand the critical rate of rise of on-state current rating is obtained from the post-test measurements.

Specified conditions

The values of the following conditions shall be stated:

a) rate of rise of on-state current di/dt;

b) peak value of on-state current; preferably twice the maximum rated mean on-state cu at the specified case or reference point temperature;

c) off-state voltage;

d) case or reference point temperature;

e) repetition rate and number of pulses;

f) gate-trigger source characteristics;

g) post-test measurement limits.

9.3.6 Peak case non-rupture current (I_{RSMC})

Purpose

To verify the peak case non-rupture current of a thyristor under specified conditions.

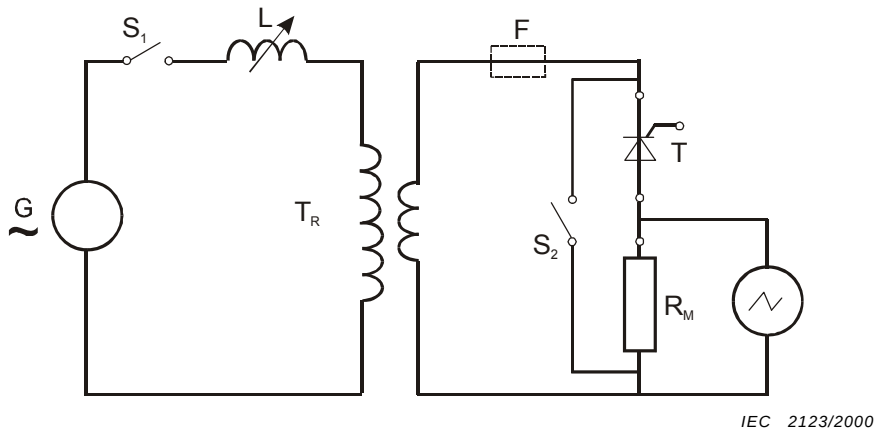


Figure 85 – Circuit diagram for measuring peak case non-rupture current

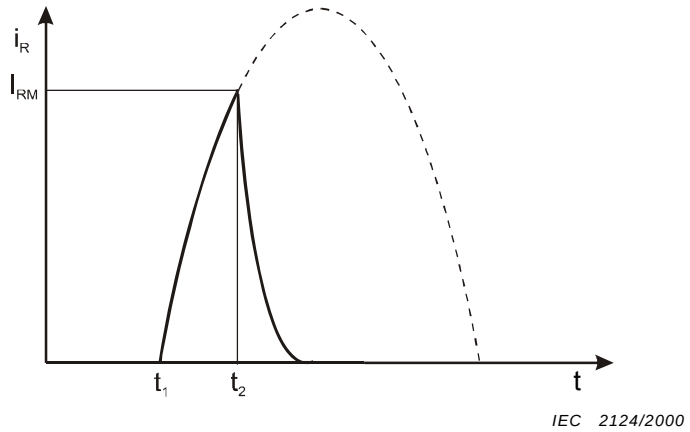


Figure 86 – Waveform of the reverse current i_R through the thyristor under test

Circuit description and requirements

G a.c. system having appropriate short-circuit capacity

S_1, S_2 electromechanical or electronic high-power switches that can be operated at defined instants of the line voltage cycle

F optional fuse in place of S_2 (see test procedure)

L variable inductor

T_R high-power transformer

RM calibrated non-inductive current-sensing resistor

T thyristor under test

Preconditioning and initial measurements

Prior to the test, the thyristor under test shall be initially damaged, for example, with a low-energy high-voltage pulse or mechanically, so that the breakdown always occurs at the edge of the silicon chip.

NOTE If required, mechanical damage can be carried out before the device is encapsulated.

The device under test is subjected to an initial leak test and the leak rate shall be lower than 10^{-7} Pa m^3s^{-1}.

Test procedure

The device under test is inserted in the test apparatus.

The switch S_1 is closed at an instant t_1 such that a voltage is applied to the device under test in the reverse direction causing a breakdown at the previously damaged spot. As a result, the reverse current rises steeply with a rate of rise that may be adjusted (within reasonable limits) by varying the inductance L.

At the instant t_2, the switch S_2 is closed so that the peak current is limited to the specified value I_{RM}.

Alternatively, fuse F may be placed in the circuit and the current through the thyristor under test will be interrupted when the fuse operates.

Specified conditions

a) case or reference point temperature;

b) value I_{RM} of the peak case non-rupture current;

c) rate of rise of the reverse current, preferably 25 A/μs;

d) pulse duration of the test current;

e) open gate circuit.

Post-test measurements

The thyristor under test is subjected to leak test and the leak rate shall be lower than 10^{-7} Pa m^3s^{-1}.

Alternatively, a plasma detecting device may be used during the electrical test to make sure that no plasma escapes during the test even if a small crack develops.

Following the electrical test, the thyristor is visually inspected. There shall be no sign of particles thrown off nor shall there be evidence that the device has externally melted or burst into flames.

9.4 Endurance tests

General requirements

Clause 2 of IEC 60747-1, chapter VIII, section three is applicable.

Specific requirements

9.4.1 List of endurance tests

For reverse-blocking triode thyristors, a choice of endurance tests is given in table 4.

9.4.2 Conditions for endurance tests

Test conditions and test circuits are listed in table 4. The relevant specification shall state which test(s) applies (apply).

9.4.3 Failure criteria and failure-defining characteristics for acceptance tests

Failure-defining characteristics, their failure criteria and measurement conditions are listed in table 3.

NOTE Characteristics should be measured in the sequence in which they are listed in table 3, because any changes in characteristics caused by certain failure mechanisms may be wholly or partially masked by the influence of other measurements.

A thyristor is also considered to have failed a test if it looses its ability to block specified voltage during the test.

9.4.4 Failure-defining characteristics and failure criteria for reliability tests

Under consideration.

9.4.5 Procedure in case of a testing error

When a device has failed as a result of a testing error (such as a test equipment fault or measurement equipment fault, or an operator error), the failure shall be noted in the data record with an explanation of the cause.

Table 3 – Failure-defining characteristics for acceptance after endurance tests

Failure-defining characteristics	Failure criteria*	Measurement conditions
I_R	> 2 × USL	Highest V_R (= V_{RRM}) and highest temperature specified for I_R
I_D	> 2 × USL	Highest V_D (= V_{DRM}) and highest temperature specified for I_D
I_{GT}	> 1,1 × USL	Lowest V_D specified for I_{GT}
V_T	> 1,1 × USL	Highest I_T specified for V_T
* USL = upper specification limit.		

Table 4 – Conditions for the endurance tests

Tests	Operating conditions			Test circuits	Remarks
	Current	Voltage	Temperature		
Operating life (resistive load)	See 2.1.5 of IEC 60747-1, chapter VIII, section three	Sine wave 50 Hz or 60 Hz Peak value = 100 % V_{RWM} or V_{DWM}	See 2.1.3. of IEC 60747-1, chapter VIII, section three		R_G = gate resistor R_L = load resistor (see note 1)
High-temperature a.c. blocking		Sine wave 50 or 60 Hz. Peak value = V_{RWM} or V_{DWM} whichever is the lower	Highest temperature for which V_{RWM} and V_{DWM} are rated		R_S = current-limiting resistor R_G = gate resistor
Thermal cycling load test	I_T (half sine wave 50 Hz or 60 Hz) must be high enough to heat the device to T_{vjmax} (see note 2)	Depends on I_T and R_L	See note 2		R_L shall be approximately equal to the effective resistance of the thyristor under test R_G= gate resistor

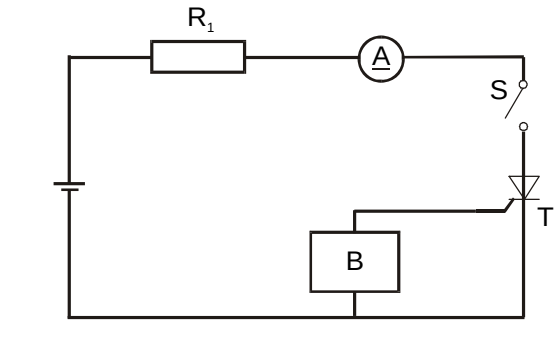
NOTE 1 Alternatively, a cheater circuit may be used.

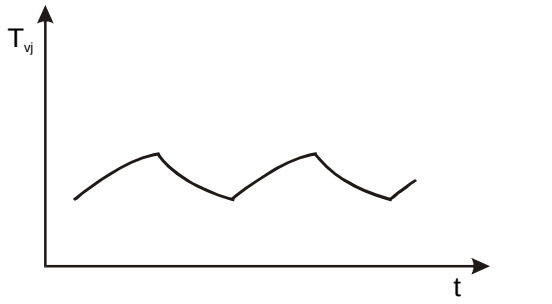
NOTE 2 See also 9.4.6.

9.4.6 Thermal cycling load test

Purpose

To confirm by an endurance test that a certain thyristor type is capable of withstanding fluctuations in junction temperature.





B gate source

T thyristor under test

Figure 87a – Test circuit **Figure 87b – Test waveform**

Figure 87 – Test circuit and test waveform for thermal cycling load test

Test procedure

The thyristor shall be heated by a specified current, the value of which is preferably nearly equal to the maximum rated mean on-state current, until a junction temperature between the maximum rated virtual junction temperature T_{vjmax} and (T_{vjmax} – 20 °C) has been reached.

NOTE When devices are tested in series, the temperature may be between T_{vjmax} and (T_{vjmax} – 30 °C).

Switch S is then opened, and the thyristor is cooled to a virtual junction temperature not greater than 40 °C.

The heating time shall not exceed 6 min and the cooling time shall not exceed 8 min.

The test shall be performed for a specified number of cycles.

The parameters that may be affected by the test shall be measured before and after the test.

Commonly specified parameters are on-state voltage, off-state current, blocking stability under stated voltage and temperature conditions, gate-trigger current and/or voltage and thermal resistance.

Annex A
(informative)

Calculation of the temperature rise under time-varying load

The load capability of semiconductor devices depends on the thermal response of the junction temperature. To calculate the rise of the virtual junction temperature caused by single load pulses or intermittent load, the transient thermal impedance can be used. As the transient thermal impedance:

$$Z_{th}(t) = \frac{\Delta T_{vj}(t)}{P}$$

is defined as the quotient of the change of the virtual junction temperature with time ($\Delta T_{vj}(t)$), and the step function change of power dissipation P causing it, the calculations are correct only for a load current which also changes as a step function. If pulses are shaped differently, a staircase approximation can be used as shown in figure A.1 below.

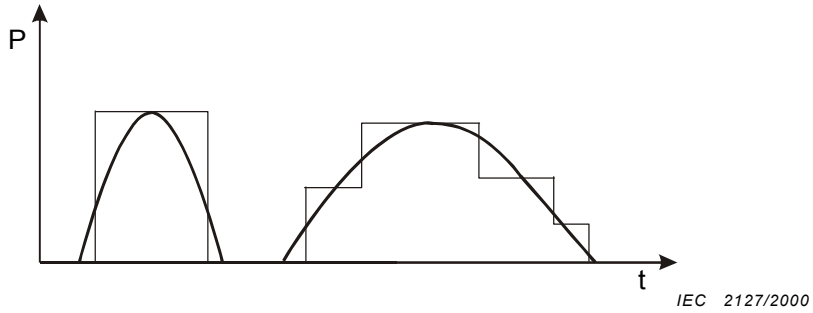


Figure A.1 – Staircase approximation for non-rectangular pulses

For the calculation of the rise of the virtual junction temperature $\Delta T_{vj}(t)$ the following two methods can be used:

Method A using the transient thermal impedance $Z_{th}(t)$:

$$\Delta T_{vj} = P \cdot Z_{th}(t)$$

Method B using an analytical function:

$$\Delta T_{vj}(t) = P \sum_{i=1}^{n} R_i \left[1 - e^{-t/\tau_i} \right]$$

representing the transient thermal impedance by a sum of terms with suitable values for R_i and τ_i.

To represent the transient thermal impedance of a semiconductor device with its cooling attachment, n equals three to six terms may be satisfactory.

As shown in the examples, it is convenient to use method A for the calculation of temperature rise caused by single pulses. For more complicated problems, e.g. in the case of an infinite sequence of pulses and varying parameters, or for more precise calculations, method B is more appropriate.

All computations are based on the superposition of thermal responses to single load pulses. An upward step of power loss will be taken as positive, a downward step as negative.

This is shown by the following typical examples.

a) Example 1: Rectangular pulse (see figure A.2 below).

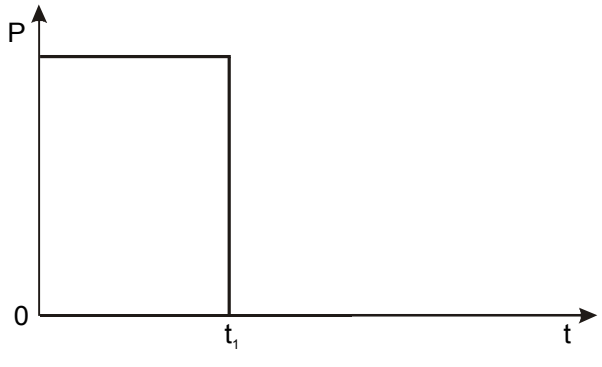


Figure A.2 – Rectangular pulse of duration t_1 producing the power dissipation P in the semiconductor device

Method A

Rise of the virtual temperature at time t_1:

$$\Delta T_{vj}(t_1) = P \cdot Z_{th}(t_1)$$

During cooling, at a time $t_2 \geq t_1$:

$$\Delta T_{vj}(t_2) = P[Z_{th}(t_2) - Z_{th}(t = t_2 - t_1)]$$

The values of $Z_{th}(t_1)$, $Z_{th}(t_2)$ and $Z_{th}(t = t_2 - t_1)$ are taken from a curve as shown in figure A.3 below.

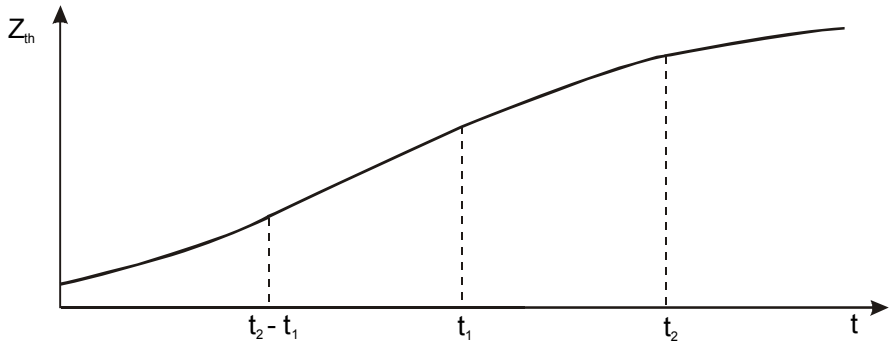


Figure A.3 – Transient thermal impedance $Z_{th}(t)$ versus time

Method B

Rise of the virtual temperature at time t_1:

$$\Delta T_{vj}(t_1) = P\sum_{i=1}^{n} R_i \left[1 - e^{-t_1/\tau_i}\right]$$

During cooling, at a time $t_2 \geq t_1$:

$$\Delta T_{vj}(t_2) = P\sum_{i=1}^{n} R_i \left[1 - e^{-t_1/\tau_i}\right] e^{-(t_2 - t_1)/\tau_i}$$

This expression can be transformed into

$$\Delta T_{vj}(t_2) = P\left\{ \sum_{i=1}^{n} R_i \left[1 - e^{-t_2/\tau_i}\right] - \sum_{i=1}^{n} R_i \left[1 - e^{-(t_2 - t_1)/\tau_i}\right] \right\}$$

This result is identical with that of method A.

b) Example 2: Single sequence of pulses (see figure A.4 below)

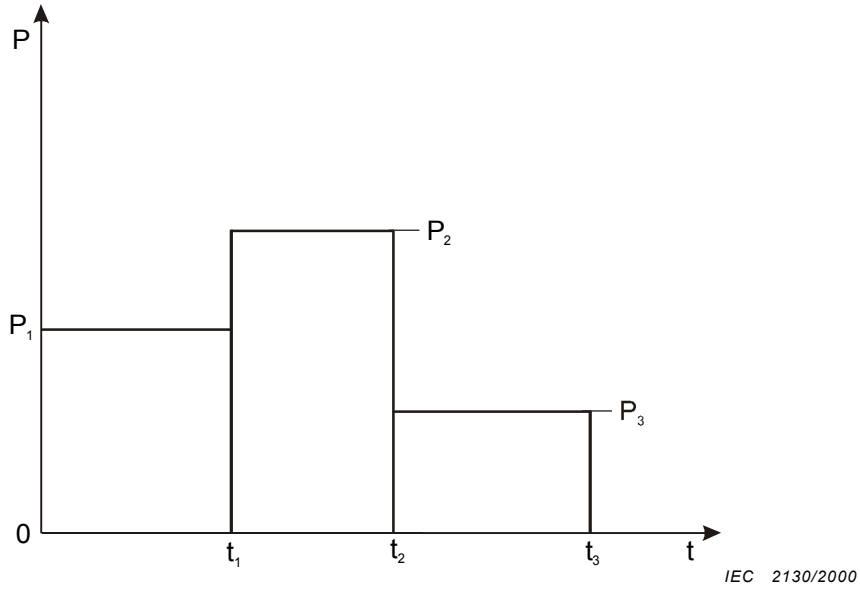


Figure A.4 – Single sequence of three rectangular pulses

From the calculation given in example 1 for the times t_1, t_2 and t_3, the following results for the virtual temperature are obtained:

Method A

$$\Delta T_{vj}(t_1) = P_1 \cdot Z_{th}(t_1)$$
$$\Delta T_{vj}(t_2) = P_1 \cdot Z_{th}(t_2) + (P_2 - P_1) \cdot Z_{th}(t = t_2 - t_1)$$
$$\Delta T_{vj}(t_3) = P_1 \cdot Z_{th}(t_3) + (P_2 - P_1) \cdot Z_{th}(t = t_3 - t_1) + (P_3 - P_2) Z_{th}(t = t_3 - t_2)$$

Method B

$$\Delta T_{vj}(t_1) = P_1 \sum_{i=1}^{n} R_i \left[1 - e^{-t_1/\tau_i}\right]$$

$$\Delta T_{vj}(t_2) = P_1 \sum_{i=1}^{n} R_i \left[1 - e^{-t_2/\tau_i}\right] + (P_2 - P_1) \sum_{i=1}^{n} R_i \left[1 - e^{-(t_2 - t_1)/\tau_i}\right]$$

$$\Delta T_{vj}(t_3) = P_1 \sum_{i=1}^{n} R_i \left[1 - e^{-t_3/\tau_i}\right] + (P_2 - P_1) \sum_{i=1}^{n} R_i \left[1 - e^{-(t_3 - t_1)/\tau_i}\right] + (P_3 - P_2) \sum_{i=1}^{n} R_i \left[1 - e^{-(t_3 - t_2)/\tau_i}\right]$$

Method A and method B give identical results.

The result remains correct, when $P_2 = 0$ (a no-load interval of duration $t_2 - t_1$ occurs).

For any sequence of Q rectangular pulses (i.e. figure A.4 continued), one finds:

for *method A*:

$$\Delta T_{vj}(t_Q) = \sum_{q=1}^{Q} (P_q - P_{q-1}) \cdot Z_{th}(t = t_Q - t_{q-1})$$

and for *method B:*

$$\Delta T_{vj}(t_Q) = \sum_{q=1}^{Q} (P_q - P_{q-1}) \cdot \sum_{i=1}^{n} R_i \left[1 - e^{-(t_Q - t_{q-1})/\tau_i}\right]$$

where $P_0 = 0$ and $t_0 = 0$.

c) Example 3: Periodic sequence of identical pulses (see figure A.5 below)

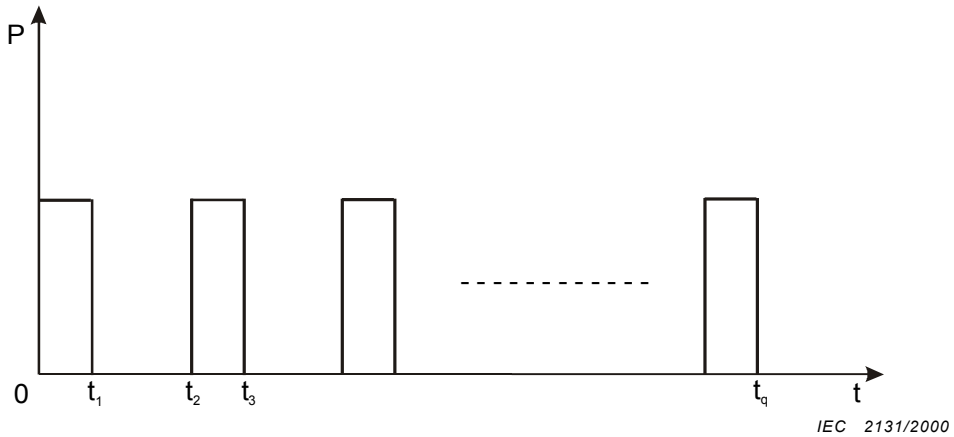


Figure A.5 – Periodic sequence of identical pulses

Method A

An approximation is recommended. Starting from a mean temperature ΔT_{vjm} caused by the mean power loss $P \cdot t_1/t_2$:

$$\Delta T_{vjm} = \frac{t_1}{t_2} P \cdot Z_{th}\left(t_\infty\right)$$

the thermal response of two consecutive pulses $\Delta T_{vj}(t_3)$ is calculated:

$$\Delta T_{vj}\left(t_3\right) = \left[1 - \frac{t_1}{t_2}\right] P \cdot Z_{th}\left(t = t_2 + t_1\right) - P \cdot Z_{th}\left(t_2\right) + P \cdot Z_{th}\left(t_1\right)$$

The total is as follows:

$$\Delta T_{vj} = \Delta T_{vjm} + \Delta T_{vj}\left(t_3\right)$$

This gives a good approximation, if one of the following conditions is fulfilled:

1) $Z_{th}\left(t_1\right) \geq 0{,}5 \cdot Z_{th}\left(t_\infty\right)$

2) $Z_{th}\left(t_2\right) - Z_{th}\left(t_1\right) \leq 0{,}1 \cdot Z_{th}\left(t_\infty\right)$

Method B

An exact calculation for the temperature rise at the end of the q^{th} pulse gives

$$\Delta T_{vj}\left(t_q\right) = P \sum_{i=1}^{n} R_i \frac{1 - e^{-t_1/\tau_i}}{1 - e^{-t_2/\tau_i}} \left[1 - e^{-qt_2/\tau_i}\right]$$

For the steady-state, i.e. when q goes to infinity (which always occurs at the end of the pulses):

$$\Delta T_{vj} = P \sum_{i=1}^{n} R_i \frac{1 - e^{-t_1/\tau_i}}{1 - e^{-t_2/\tau_i}}$$

d) Example 4: Load by a periodic sequence of various pulses, e.g. according to figure A.6 below

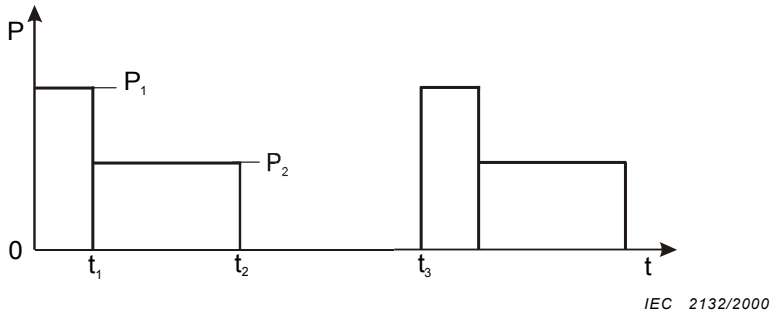


Figure A.6 – Periodic sequence, each consisting of two different pulses

Method A

An approximation similar to example 3 is recommended. Starting from the mean temperature rise:

$$\Delta T_{vjm} = \frac{1}{t_3}\left[t_1 P_1 + (t_2 - t_1)P_2\right] \cdot Z_{th}(t_\infty)$$

the thermal response $\Delta T_{vj}(t = t_3 + t_2)$ is calculated:

$$\Delta T_{vj}(t = t_3 + t_2) = \left[P_1 - \frac{1}{t_3}\{t_1 P_1 + (t_2 - t_1)P_2\}\right] \cdot Z_{th}(t = t_3 + t_2) - \\ - (P_1 - P_2) \cdot Z_{th}(t = t_3 + t_2 - t_1) - P_2 - Z_{th}(t_3) + \\ + (P_1) \cdot Z_{th}(t_2) + (P_1 - P_2) \cdot Z_{th}(t = t_2 - t_1)$$

The total is then

$$\Delta T_{vj} = \Delta T_{vjm} + \Delta T_{vj}(t = t_3 + t_2)$$

Method B

An exact calculation for the temperature rise in the q^{th} sequence is possible:

$$\Delta T_{vj}(q \cdot t_3) = P_1 \sum_{i=1}^{n} R_i \frac{\left[1 - e^{-t_1/\tau_i}\right] e^{-(t_2 - t_1)/\tau_i} \left[1 - e^{-qt_3/\tau_i}\right]}{1 - e^{-t_3/\tau_i}} + \\ + P_2 \sum_{i=1}^{n} R_i \frac{1 - e^{-(t_2 - t_1)/\tau_i}}{1 - e^{-t_3/\tau_i}} \left[1 - e^{-qt_3/\tau_i}\right]$$

For the steady state, i.e. when q goes to infinity (which always occurs at the end of the second pulse):

$$\Delta T_{vj} = P_1 \sum_{i=1}^{n} R_i \frac{\left[1 - e^{-t_1/\tau_i}\right] e^{-(t_2 - t_1)/\tau_i}}{1 - e^{-t_3/\tau_i}} + P_2 \sum_{i=1}^{n} R_i \frac{1 - e^{-(t_2 - t_1)/\tau_i}}{1 - e^{-t_3/\tau_i}}$$

e) Additional superpositions

For all examples additional superpositions can be considered if the thyristor is operated at switching frequencies below 200 Hz.

Two cases are to be distinguished:

1) Steady-state load. In this case, the calculated temperature rise ΔT_{vj} is superimposed to a steady-state temperature rise ΔT_{vjst}:

$$\Delta T_{vjst} = P_{st} \cdot Z_{th}(t_\infty) = P_{st} \cdot \sum_{i=1}^{n} R_i$$

where P_{st} is the steady-state power dissipation. The calculated temperature rise is then:

$$\Delta T_{vjst} + \Delta T_{vj}$$

2) Load pulses. Every load pulse can consist of a pulse sequence of higher frequency. e.g. line frequency. In this case, an additional oscillation of the virtual junction temperature occurs. To calculate the maximum of this temperature oscillation, an additional term is required. This term can be derived from example 3.

Method A

The required term is formed in the same manner as $\Delta T_{vj}(t_3)$ in example 3.

Method B

The constants R_i can be replaced by R_i':

$$R_i' = R_i \frac{1 - e^{-t_1 / \tau_i}}{1 - e^{-t_2 / \tau_i}}$$

where t_1 is the pulse duration and t_2 the reciprocal repetition rate of the higher frequency.

Table A.1 – Equations for calculating the virtual junction temperature rise for some typical load variations

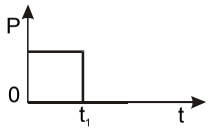
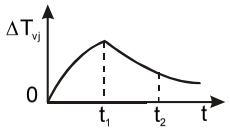
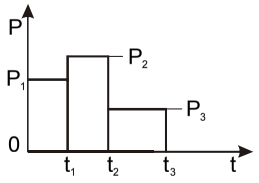
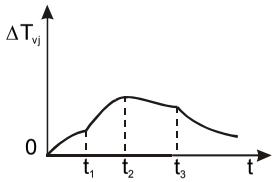
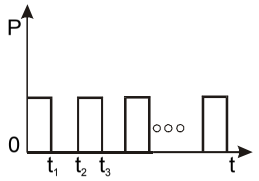
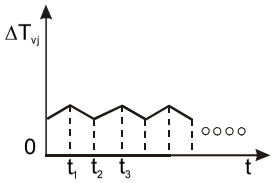
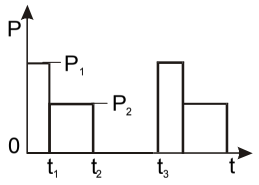
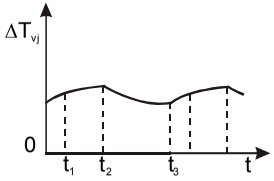
Load condition	Thermal response	Calculation methods	
		Method A	**Method B**
Single pulse 		$\Delta T_{vj}(t_1) = P \cdot Z_{th}(t_1)$ $\Delta T_{vj}(t_2) = P \cdot Z_{th}(t_2) - P \cdot Z_{th}(t = t_2 - t_1)$	$\Delta T_{vj}(t_1) = P \cdot \sum_{i=1}^{n} R_i \left[1 - e^{-t_1/\tau_i}\right]$ $\Delta T_{vj}(t_2) = P \cdot \sum_{i=1}^{n} R_i \left[1 - e^{-t_2/\tau_i}\right] -$ $- P \cdot \sum_{i=1}^{n} R_i \left[1 - e^{-(t_2 - t_1)/\tau_i}\right]$
Single sequence of three pulses 		$\Delta T_{vj}(t_1) = P_1 \cdot Z_{th}(t_1)$ $\Delta T_{vj}(t_2) = P_1 \cdot Z_{th}(t_2) +$ $+ (P_2 - P_1) \cdot Z_{th}(t = t_2 - t_1)$ $\Delta T_{vj}(t_3) = P_1 \cdot Z_{th}(t_3) +$ $+ (P_2 - P_1) \cdot Z_{th}(t = t_3 - t_1) +$ $+ (P_3 - P_2) \cdot Z_{th}(t = t_3 - t_2)$	$\Delta T_{vj}(t_1) = P_1 \cdot \sum_{i=1}^{n} R_i \left[1 - e^{-t_1/\tau_i}\right]$ $\Delta T_{vj}(t_2) = P_1 \cdot \sum_{i=1}^{n} R_i \left[1 - e^{-t_2/\tau_i}\right] +$ $+ (P_2 - P_1) \sum_{i=1}^{n} R_i \left[1 - e^{-(t_2 - t_1)/\tau_i}\right]$ $\Delta T_{vj}(t_3) = P_1 \cdot \sum_{i=1}^{n} R_i \left[1 - e^{-t_3/\tau_i}\right] +$ $+ (P_2 - P_1) \cdot \sum_{i=1}^{n} R_i \left[1 - e^{-(t_3 - t_1)/\tau_i}\right] +$ $+ (P_3 - P_2) \cdot \sum_{i=1}^{n} R_i \left[1 - e^{-(t_3 - t_2)/\tau_i}\right]$
Single sequence of Q pulses $P_0 = 0 \quad t_0 = 0$		$\Delta T_{vj}(t_Q) = \sum_{q=1}^{Q} (P_q - P_{q-1}) \cdot Z_{th}(t = t_Q - t_{q-1})$	$\Delta T_{vj}(t_Q) = \sum_{q=1}^{Q} (P_q - P_{q-1}) \cdot \sum_{i=1}^{n} R_i \left[1 - e^{-(t_Q - t_{q-1})/\tau_i}\right.$

Table A.1 *(continued)*

Load condition	Thermal response	Calculation methods	
		Method A	**Method B**
Periodical sequence of homogeneous pulses 		$\Delta T_{vj} = \Delta T_{vjm} + \Delta T_{vj}(t_3)$ $\Delta T_{vjm} = \frac{t_1}{t_2} P \cdot Z_{th}(t_\infty)$ $\Delta T_{vj}(t_3) = (1 - \frac{t_1}{t_2}) P \cdot Z_{th}(t = t_2 + t_1) -$ $- P \cdot Z_{th}(t_2) + P \cdot Z_{th}(t_1)$	$\Delta T_{vj} = P \cdot \sum_{i=1}^{n} R_i \frac{1 - e^{-t_1/\tau_i}}{1 - e^{-t_2/\tau_i}}$
Periodical sequence, each consisting of two different pulses 		$\Delta T_{vj} = \Delta T_{vjm} + \Delta T_{vj}(t = t_3 + t_2)$ $\Delta T_{vjm} = \frac{1}{t_3}[t_1 P_1 + (t_2 - t_1) P_2] \cdot Z_{th}(t_\infty)$ $\Delta T_{vj}(t = t_3 + t_2) = \left[P_1 - \frac{1}{t_3}\{t_1 P_1 + (t_2 - t_1) P_2\}\right] \cdot$ $Z_{th}(t = t_3 + t_2) -$ $-(P_1 - P_2) \cdot Z_{th}(t = t_3 + t_2 - t_1) -$ $-P_2 \cdot Z_{th}(t_3) + P_1 \cdot Z_{th}(t_2) +$ $+(P_1 - P_2) Z_{th}(t = t_2 - t_1)$	$\Delta T_{vj} = P_1 \cdot \sum_{i=1}^{n} R_i \frac{\left(1 - e^{-t_1/\tau_i}\right) \cdot e^{-(t_2 - t_1)/\tau_i}}{1 - e^{-t_3/\tau_i}} +$ $+ P_2 \cdot \sum_{i=1}^{n} R_i \frac{1 - e^{-(t_2 - t_1)/\tau_i}}{1 - e^{-t_3/\tau_i}}$